Alveo UL3524 Ultra Low Latency Trading Data Sheet

DS1009 (v1.1.1) November 21, 2023 **Product Specification**

Summary

The AMD Alveo™ UL3524 card is designed for ultra low latency applications for the fintech market. It consists of an AMD UltraScale+™ device with ultra-low latency GTF transceivers, QDR, and DDR memory. In addition, it has four QSFP-DD NIC ports supporting 32 GTF TX/RX pairs along with high-speed expansion connectors supporting 32 additional GTF TX/RX pairs.

The UL3524 is a full height, ¾ length, single slot PCIe® CEM 4.0 compliant card which supports passive cooling for closed-loop thermal control in the server PCIe expansion slot. It has a PCIe x16 physical connector with the upper eight lanes unconnected.

The card supports both appliance and PCIe power modes:

- In appliance mode, all power is drawn from the PCIe 12V AUX power connector.
- In PCIe power mode, power is drawn from both the PCIe 12 AUX power connector and the PCIe 12V edge connector.

The following figure shows the UL3524 card.

Figure 1: **UL3524 Card**

Designs can be developed with the AMD Vivado™ Design Suite where the full resources of the programmable logic device are made available for development.

Product Details

The following table lists high-level product details for the UL3524 card.

Table 1: **Alveo UL3524 Product Details**

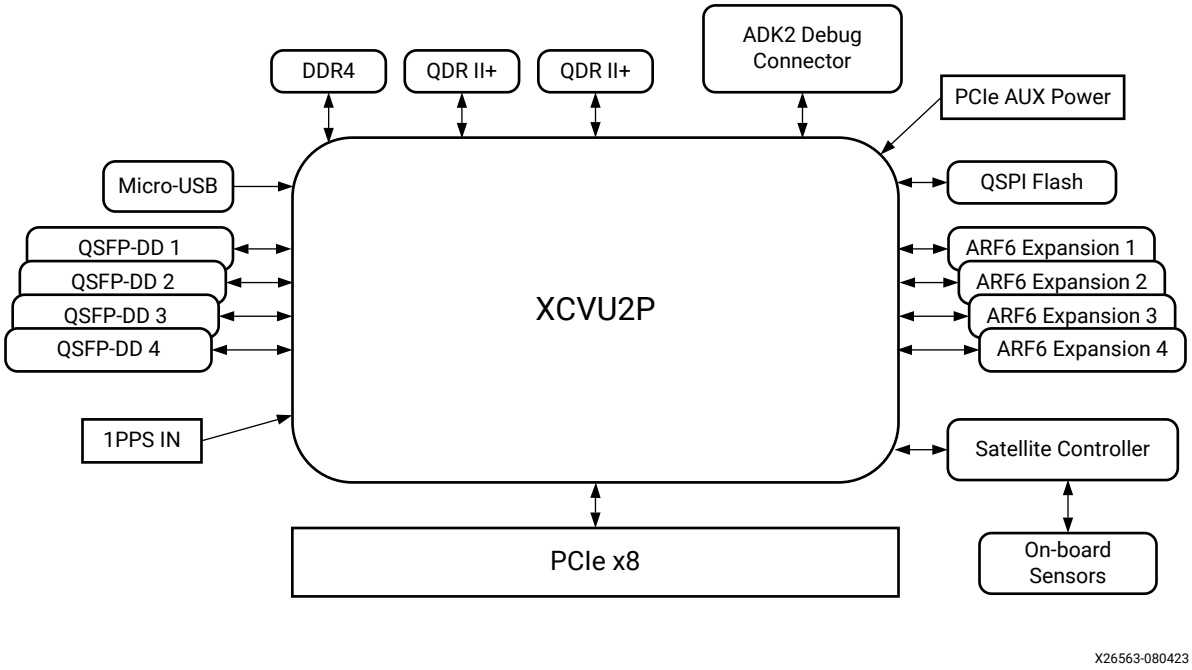
Specification	UL3524
Product SKU	A-UL3524-P16G-PQ-G
Total electrical card load - PCIe Mode	180W
Total electrical card load - Appliance Mode	150W
Thermal design power (TDP)	125W
Thermal cooling solution	Passive
Weight	832g
Form factor	Full-height, ¾ length, single slot
Network interface	Four QSFP-DD
PCIe interface	PCIe Gen4 x8
Expansion ports	Four ARF6 + two PicoClasp for sideband
QDR II+	72 MB 2 x 288 Mb QDR II+, 550 MHz
DDR4	16 GB 64b + 8b ECC at 2666 MT/s
1 PPS	1PPS IN port
Qualified for deployment	Yes
Vivado tools part number	XCVU2P-FSVJ2104-3-E
Card management	External SC MSP432P4011IRGCT
Power management	Power management with power management bus (PMBus) for voltage, current, and temperature monitoring including telemetry for major regulators
External power source	12V PCIe AUX 2x4
ADK2 Enabled	Yes
Configuration option	• 2 Gbit QSPI • JTAG over Micro-USB or ADK2
Debug interface	• UARTs over Micro-USB • PMBus, SMBus over ADK2 Debug Connector
Card security	None

Card Specifications

Block Diagram

The high-level block diagram for the UL3524 card is given in the following figure.

Figure 2: **UL3524 High-Level Block Diagram**

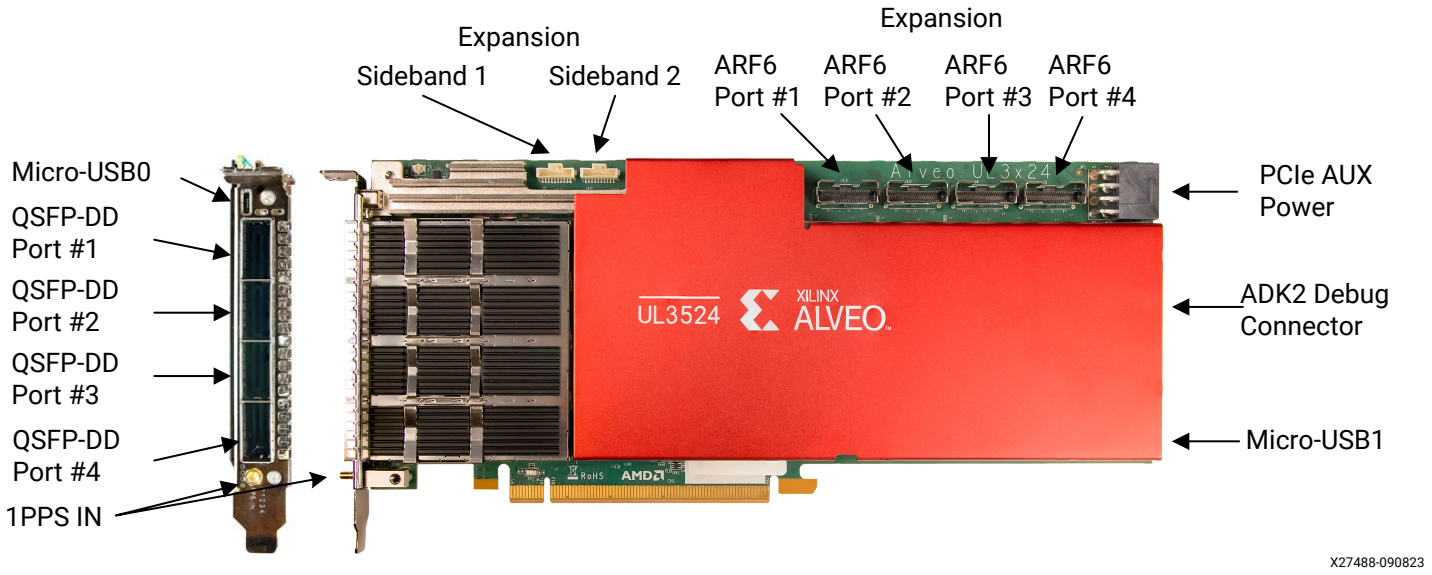


Card Interfaces

The Alveo UL3524 card is available in a passive cooling configuration and is designed for installation into a data center server where controlled air flow provides direct cooling to the card. The following figure shows the Alveo UL3524 card, including the following interfaces:

- A PCIe card connector
- Four QSFP-DD NIC ports supporting 32 GTF TX/RX lanes
- Four ARF6 connectors supporting 32 GTF TX/RX lanes
- Micro-USB maintenance connector
- ADK2
- AUX power connector

Figure 3: **UL3524 Card Interfaces**



Note: Block diagrams, register maps, and the XDC file reference the QSFP-DD ports as QSFP-DD0 through QSFPDD3. These references map to the card QSFP-DD labeling Port #1 through Port #4, see Network Port Labels for details.

FPGA Resources

The UL3524 card is populated with the AMD XCVU2P-3FSVJ2104E FPGA. The high-level FPGA resources for this device are given in the following table.

Table 2: **Available FPGA Resources**

Specification	Resources
System logic cells (K)	1722
LUTs (K)	787
BRAM (Mbits)	76
URAM (Mbits)	180
HPIO	416
HDIO	48
GTYP transceivers	8
GTF transceivers	72[1]
PCIE4C Gen4 x8	1
Package, mm	47.5 x 47.5/1 mm ball pitch
Speed grade	-3

Notes:

1. While the FPGA has 72 GTF transceivers, only 64 are used by the card.

FPGA Bank I/O Mapping

The following figure and associated table give the FPGA bank I/O allocation along with additional details including assigned function and VCCO allocation. Both HDIO (high density I/O) and HPIO (high performance I/O) banks are used. Allocation of bank type is dependent on the required function (i.e., memory interface or UART). Dedicated Bank 0 is allocated for JTAG and configuration QSPI interface, and it is not detailed in the table.

Figure 4: **FPGA Bank Allocation**

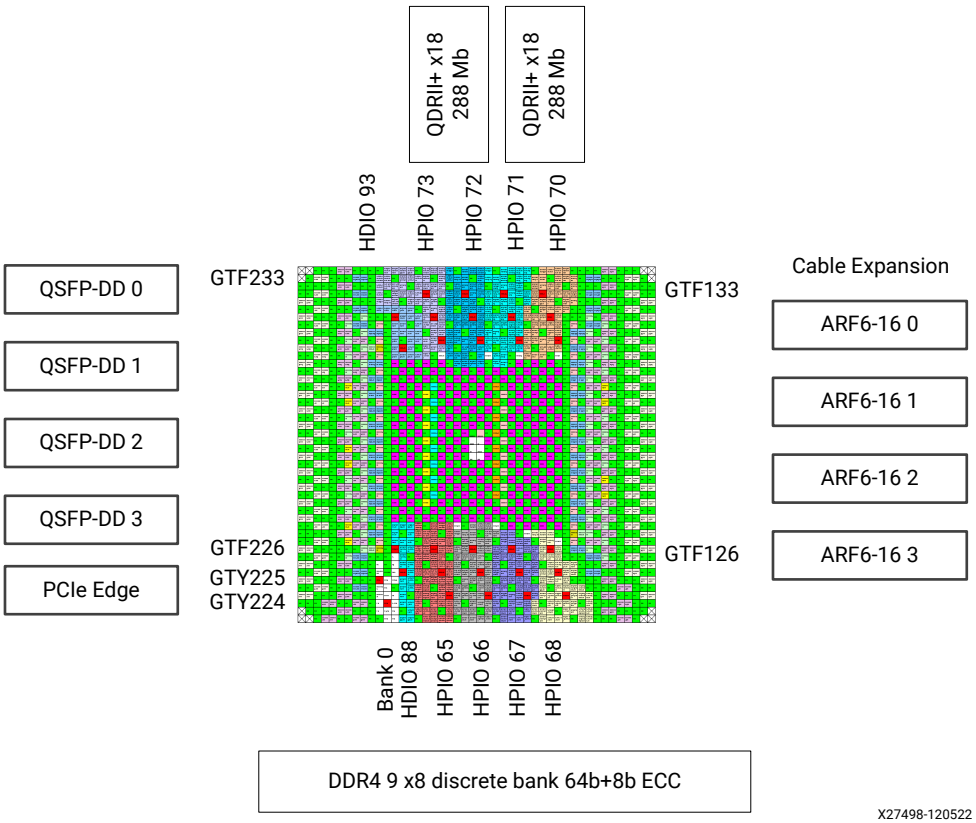


Table 3: **FPGA Bank Allocation**

FPGA Bank	Bank Type	Function(s)	VCCO
65	HPIO	• RX recovered clocks • EMCCLK	1.8
66 - 68	HPIO	DDR4 Controller	1.2
70 - 71	HPIO	QDR-II+ Controller 1	1.5
72 - 73	HPIO	QDR-II+ Controller 0	1.5
88	HDIO	• Three UARTs • QSFP-DD LEDs • PPS IN	3.3
93	HDIO	• Expansion Sideband 1 & 2 • QSFP-DD Sideband	3.3

Table 3: **FPGA Bank Allocation** *(cont'd)*

FPGA Bank	Bank Type	Function(s)	VCCO
126 - 127	GTF	ARF6 3 Expansion Connector • TX / RX 1-4 assigned to bank 127 • TX / RX 5-8 assigned to bank 126	N/A
128- 129	GTF	ARF6 2 Expansion Connector • TX / RX 1-4 assigned to bank 129 • TX / RX 5-8 assigned to bank 128	N/A
130 - 131	GTF	ARF6 1 Expansion Connector • TX / RX 1-4 assigned to bank 131 • TX / RX 5-8 assigned to bank 130	N/A
132 - 133	GTF	ARF6 0 Expansion Connector • TX / RX 1-4 assigned to bank 133 • TX / RX 5-8 assigned to bank 132	N/A
224 - 225	GTY	PCIe x8 to Edge Connector • PCIe Lane 3-0 on bank 225 • PCIe Lane 7-4 on bank 224 • Upper 8 lanes of PCIe x16 connector are not connected.	N/A
226 - 227	GTF	QSFP-DD 3 • TX / RX 1-4 assigned to bank 227 • TX / RX 5-8 assigned to bank 226	N/A
228 - 229	GTF	QSFP-DD 2 • TX / RX 1-4 assigned to bank 228 • TX / RX 5-8 assigned to bank 229	N/A
230 - 231	GTF	QSFP-DD 1 • TX / RX 1-4 assigned to bank 230 • TX / RX 5-8 assigned to bank 231	N/A
232 - 233	GTF	QSFP-DD 0 • TX / RX 1-4 assigned to bank 232 • TX / RX 5-8 assigned to bank 233	N/A

I2C Register Map

The following table provides the I2C base address register map for accessible devices. Registers are grouped under similar areas, and their accessibility (from FPGA, BMC, or SC) is noted. For I2C register details, see the manufacturer's respective device datasheet.

Table 4: **I2C Base Address Register Map for Accessible Devices**

	8-bit (HEX)	7-bit (HEX)		
Register Name	**Address**		**Description**	**Device**
DDR4 Power and Clocks CLKGEN_SCL / SDA—*Accessible from the FPGA only*				
Clock generator	0x12	0x09	Clock generator component	Renesas RC21008AQ
Jitter cleaner 1	0xB0	0x58	Enable QSFP-DD jitter cleaner	Renesas RC38612A002GN2

Table 4: **I2C Base Address Register Map for Accessible Devices** *(cont'd)*

	8-bit (HEX)	7-bit (HEX)		
Register Name	**Address**		**Description**	**Device**
Jitter cleaner 2	0xB2	0x59	Enable expansion ports jitter cleaner	Renesas RC38612A002GN2
DDR4 power control	0x42	0x21	Enable power to DDR4[1]	TI TCA6408PWR
QSFP-DD—*Accessible from the FPGA only*				
QSFP-DD Power Control QSFP-DD0, QSFP-DD1, QSFP-DD2, QSFP-DD3	0x42	0x21	QSFP-DD ports[1] power control	TI TCA6408APWR
QSFP-DD I/O Expander QSFP-DD0, QSFP-DD1, QSFP-DD2, QSFP-DD3	0x40	0x20	QSFP-DD ports[1] I/O expander	TI TCA6408APWR
MUX0	0xE0	0x70	See note 1.	PCA9545A
MUX1	0xE4	0x72	See note 1.	PCA9545A
ARF6 Expansion Port—*Accessible from the FPGA only*				
Expansion port I2C			Future use	
System I2C_MAIN_SCL / SDA—*Accessible from the SC only*				
EEPROM	0xA4 / 0xB4	0x52 / 0x5A	Card serial number access.	STM M24C64
FPGA thermal diode sensor	0x9C	0x4E	FPGA temperature	TI TMP411CDGKT
Temperature sensor (left)	0x90	0x48	Card outlet temperature	NXP LM75BTP
Temperature sensor (right)	0x92	0x49	Card inlet temperature	NXP LM75BTP
Power PMBUS_SCL / SDA—*Accessible from Server BMC or SC only*				
Input power monitor	0x80	0x40	Input voltage/current/power monitor for the following power rails: • 3.3V PCIe • 12V PCIe • 12V PCIe AUX	TI INA3221A
VRM controller	0xC0	0x60	Multi-rail power controller.	Renesas ISL68224IRAZ

Notes:

1. See reference designs for support details.

Card Power System

Power Modes of Operation

The card supports both appliance and PCIe® power modes of operation.

- In appliance power mode, all power is drawn from the PCIe12V AUX power connector.
- In PCIe power mode, power is drawn from both the PCIe 12V AUX power connector and the PCIe edge connector.

Power to the satellite controller (SC) is dependent on the power mode selected. Both the SC and sensor power are derived from two sources using an ORing diode schema:

- PCIe 12V AUX from edge connector.

- On-board 3.3V regulator from PCIe 12V AUX.

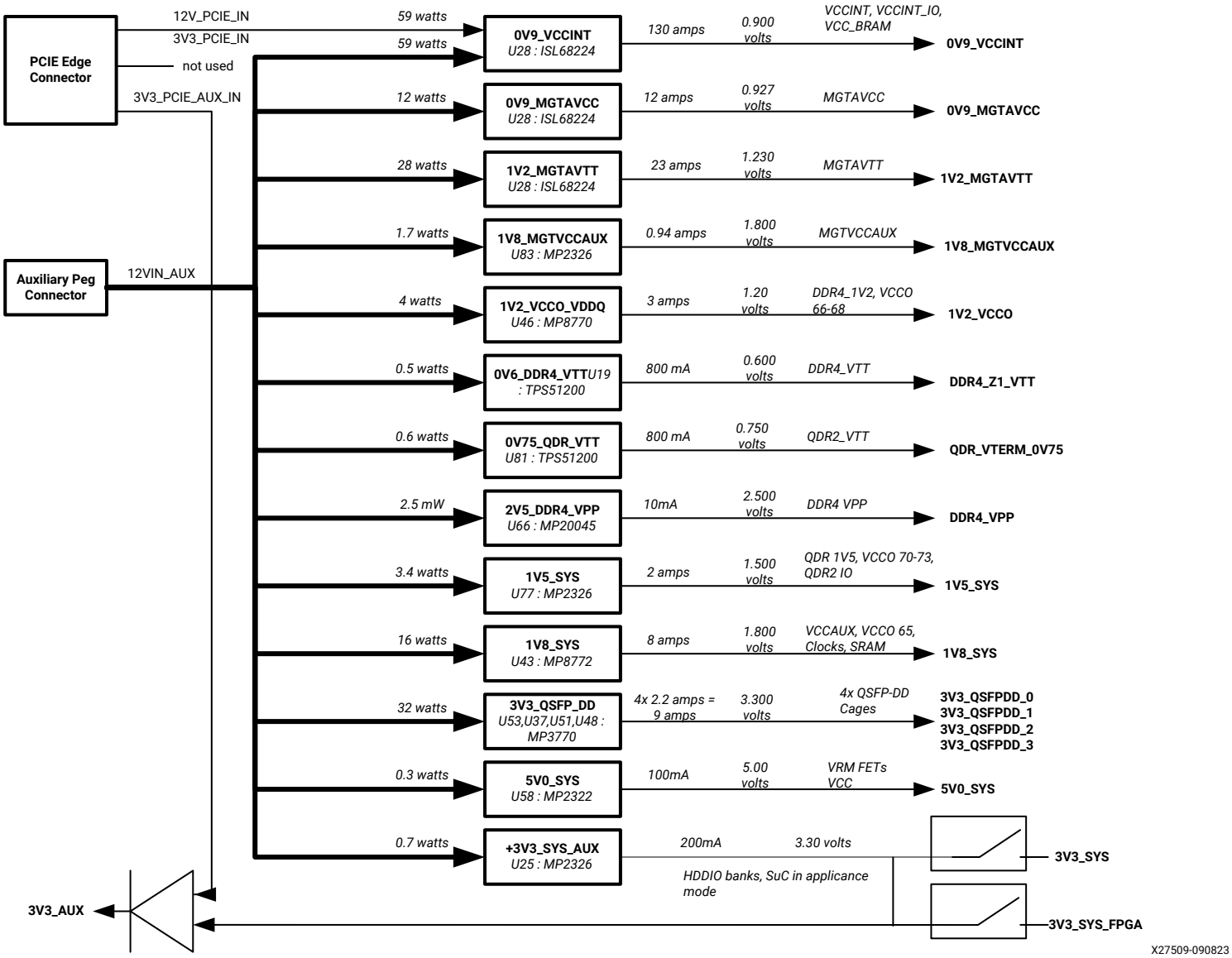
For PCIe power mode, the SC and sensors are powered from the PCIe 3.3V AUX and can support stand-by operation. For appliance power mode, the SC is not functional until the PCIe 12V AUX power is enabled.

Power Tree

The following figure shows the high-level power tree. Key details include:

- Main FPGA power is delivered by ISL68224 controller with ISL99360 power stages.
- VCCINT power is generated by two power phases, taking input power from the following:
  - PCIe 12V edge connector
  - PCIe 12V Auxiliary
- There are two main power planes from the ISL68224, with one phase per plane.
- Each QSFP-DD uses isolated power, which is delivered by a dedicated regulator that provides power enable and over-current control per port.

Figure 5: **Card Power Tree**



PCIe Connector

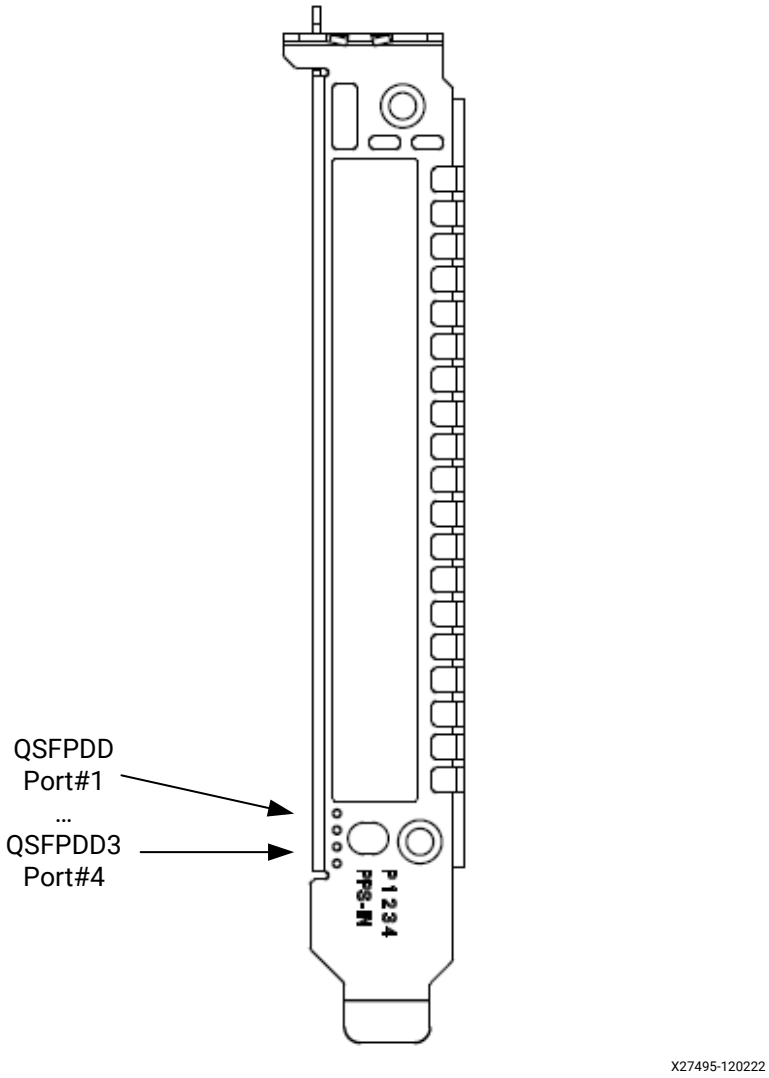
The Alveo UL3524 card has a PCIe Gen4 x8 interface compliant with PCIe CEM 4.0 configured as a PCIe Endpoint. It has a PCIe x16 physical connector with the upper eight lanes unconnected and does not support bifurcation.

For information about PCIe FPGA bank allocation and clocking details, see FPGA Bank I/O Mapping and Clocking. Detailed AMD UltraScale+™ device and PCIe pin connections can be found in the UL3524 Xilinx Design Constraints (XDC) file.

LED Indicators

The card has four QSFP-DD user-definable LEDs visible through a cutout in the PCIe® I/O bracket, as shown in the following figure.

Figure 6: **PCIe I/O Bracket LED Location**



The following table details the LED definition along with the FPGA pin.

Table 5: **Network Status LEDs**

LED Name	Description	FPGA Pin
QSFP-DD Link	User-definable green LED.	AR13 for QSFP-DD Port #1 AP13 for QSFP-DD Port #2 AP14 for QSFP-DD Port #3 AP15 for QSFP-DD Port #4

Network Interfaces

The Alveo UL3524 card hosts four 8-lane small form-factor pluggable (QSFP-DD) connectors that are housed within a ganged 1x4 QSFP-DD cage assembly with heatsink. It can be populated with QSFP or QSFP-DD direct attach copper or optical modules supporting up to 7W. The QSFP-DD can connect interfaces up to 100G using optical modules or cables. A 161.1328125 MHz clock is provided to the QSFP-DD interface such that different Ethernet IP cores can be enabled.

Network Port Labels

The QSFP-DD network ports on the card are labeled Port #1 through Port #4, with their locations shown in Figure 3.

Note: Block diagrams, register maps, and the XDC file reference the QSFP-DD ports as QSFP-DD0 through QSFPDD3. These references map to the card QSFP-DD labeling Port #1 through Port #4 as outlined in the following table. Similar labeling occurs with the ARF6 ports.

Table 6: **QSFP-DD Card Port Label to XDC / Block Diagram Net Port Label**

QSFP-DD Port Label	Net / Block Diagram Port Label
QSFP-DD Port #1	QSFP-DD0
QSFP-DD Port #2	QSFP-DD1
QSFP-DD Port #3	QSFP-DD2
QSFP-DD Port #4	QSFP-DD3

Network MAC Address

Each card has 64 contiguous MAC addresses.

Determine Allocated MAC Addresses

Use the following steps to determine the 64 allocated MAC addresses.

1. Determine the Base MAC Address
2. Use Formula to Compute Allocated MAC Addresses

Determine the Base MAC Address

To determine the base MAC address, use the Satellite Controller to display the board information, or look at a sticker on the physical card.

Use Satellite Controller to Display Board Info

Using the Satellite Controller, display *Board Info*. Board MAC0 is the base MAC address. See reference designs for support details.

Identify Base MAC Address From Sticker

On the PCIe® interface of the card, a sticker displays two MAC addresses:

- **MAC1:** Denotes the base MAC address.
- **MAC64:** Represents the last allocated MAC address.

Use Formula to Compute Allocated MAC Addresses

With the base MAC address, use the following formula to compute the 64 allocated MAC addresses.

$$MAC(i) = MAC\ base\ address + i$$

Where i is an integer from 0 to 63.

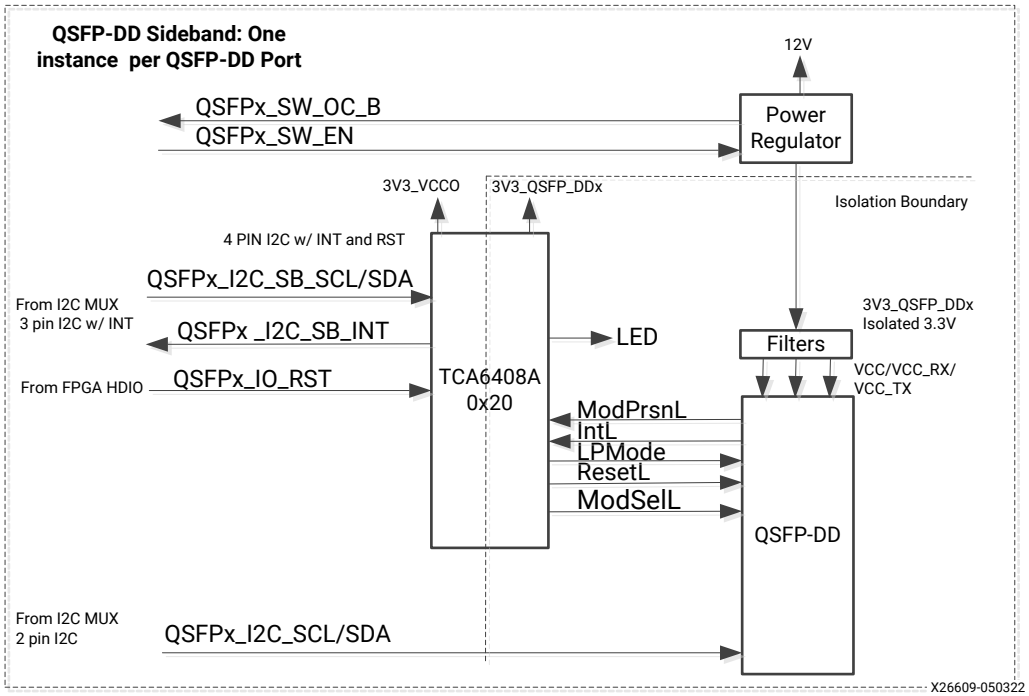
Network Port LEDs

See LED Indicators.

QSFP-DD Isolation Logic

To ensure the I2C bus is not taken down, in the case of a malfunctioning QSFP-DD module, each sideband I/O expander consists of an electrical isolation boundary and short-circuit protection logic (shown in the following image).

Figure 7: **QSFP-DD Electrical Isolation Block Diagram**



QSFP-DD Sideband Management

The QSFP-DD connector sideband signals are accessible directly from the FPGA via the I2C interface. See reference designs for support details.

QSFP-DD to GTF Lane Mapping

QSFP-DD GTF interface lane mapping and high-speed connections are detailed in the following tables. Content is also provided in the UL3524 XDC file.

QSFP-DD0 Interface Lane Mapping and High-Speed Connections

Table 7: **QSFP-DD0 Interface Lane Mapping**

Signal Name	Direction	Bank	I/O Reference	Pin	Description
SYNCE_CLK16_LVDS_N	Input	232	MGTREFCLK0N_232	H8	REFCLK0 negative LVDS signal.
SYNCE_CLK16_LVDS_P	Input	232	MGTREFCLK0P_232	H9	REFCLK0 positive LVDS signal.
SYNCE_CLK17_LVDS_N	Input	233	MGTREFCLK0N_233	D8	REFCLK0 negative LVDS signal.
SYNCE_CLK17_LVDS_P	Input	233	MGTREFCLK0P_233	D9	REFCLK0 positive LVDS signal.
QSFPDD0_RX_N[1]	Input	232	MGTFRXN0_232	K3	Negative receive lane 1 input.
QSFPDD0_RX_P[1]	Input	232	MGTFRXP0_232	K4	Positive receive lane 1 input.
QSFPDD0_RX_N[2]	Input	232	MGTFRXN1_232	J1	Negative receive lane 2 input.
QSFPDD0_RX_P[2]	Input	232	MGTFRXP1_232	J2	Positive receive lane 2 input.
QSFPDD0_RX_N[3]	Input	232	MGTFRXN2_232	H3	Negative receive lane 3 input.
QSFPDD0_RX_P[3]	Input	232	MGTFRXP2_232	H4	Positive receive lane 3 input.
QSFPDD0_RX_N[4]	Input	232	MGTFRXN3_232	G1	Negative receive lane 4 input.
QSFPDD0_RX_P[4]	Input	232	MGTFRXP3_232	G2	Positive receive lane 4 input.
QSFPDD0_RX_N[5]	Input	233	MGTFRXN0_233	F3	Negative receive lane 5 input.
QSFPDD0_RX_P[5]	Input	233	MGTFRXP0_233	F4	Positive receive lane 5 input.
QSFPDD0_RX_N[6]	Input	233	MGTFRXN1_233	E1	Negative receive lane 6 input.
QSFPDD0_RX_P[6]	Input	233	MGTFRXP1_233	E2	Positive receive lane 6 input.
QSFPDD0_RX_N[7]	Input	233	MGTFRXN2_233	D3	Negative receive lane 7 input.
QSFPDD0_RX_P[7]	Input	233	MGTFRXP2_233	D4	Positive receive lane 7 input.
QSFPDD0_RX_N[8]	Input	233	MGTFRXN3_233	B3	Negative receive lane 8 input.
QSFPDD0_RX_P[8]	Input	233	MGTFRXP3_233	B4	Positive receive lane 8 input.
QSFPDD0_TX_N[1]	Output	232	MGTFTXN0_232	M8	Negative transmit lane 1 output.
QSFPDD0_TX_P[1]	Output	232	MGTFTXP0_232	M9	Positive transmit lane 1 output.
QSFPDD0_TX_N[2]	Output	232	MGTFTXN1_232	L6	Negative transmit lane 2 output.
QSFPDD0_TX_P[2]	Output	232	MGTFTXP1_232	L7	Positive transmit lane 2 output.
QSFPDD0_TX_N[3]	Output	232	MGTFTXN2_232	K8	Negative transmit lane 3 output.
QSFPDD0_TX_P[3]	Output	232	MGTFTXP2_232	K9	Positive transmit lane 3 output.
QSFPDD0_TX_N[4]	Output	232	MGTFTXN3_232	J6	Negative transmit lane 4 output.
QSFPDD0_TX_P[4]	Output	232	MGTFTXP3_232	J7	Positive transmit lane 4 output.
QSFPDD0_TX_N[5]	Output	233	MGTFTXN0_233	G6	Negative transmit lane 5 output.
QSFPDD0_TX_P[5]	Output	233	MGTFTXP0_233	G7	Positive transmit lane 5 output.
QSFPDD0_TX_N[6]	Output	233	MGTFTXN1_233	E6	Negative transmit lane 6 output.
QSFPDD0_TX_P[6]	Output	233	MGTFTXP1_233	E7	Positive transmit lane 6 output.
QSFPDD0_TX_N[7]	Output	233	MGTFTXN2_233	C6	Negative transmit lane 7 output.
QSFPDD0_TX_P[7]	Output	233	MGTFTXP2_233	C7	Positive transmit lane 7 output.
QSFPDD0_TX_N[8]	Output	233	MGTFTXN3_233	A6	Negative transmit lane 8 output.
QSFPDD0_TX_P[8]	Output	233	MGTFTXP3_233	A7	Positive transmit lane 8 output.

QSFP-DD1 Interface Lane Mapping and High-Speed Connections

Table 8: **QSFP-DD1 Interface Lane Mapping**

Signal Name	Direction	Bank	I/O Reference	Pin	Description
SYNCE_CLK14_LVDS_N	Input	230	MGTREFCLK0N_230	U10	REFCLK0 negative LVDS signal.
SYNCE_CLK14_LVDS_P	Input	230	MGTREFCLK0P_230	U11	REFCLK0 positive LVDS signal.
SYNCE_CLK15_LVDS_N	Input	231	MGTREFCLK0N_231	N10	REFCLK0 negative LVDS signal.
SYNCE_CLK15_LVDS_P	Input	231	MGTREFCLK0P_231	N11	REFCLK0 positive LVDS signal.
QSFPDD1_RX_N[1]	Input	230	MGTFRXN0_230	V3	Negative receive lane 1 input.
QSFPDD1_RX_P[1]	Input	230	MGTFRXP0_230	V4	Positive receive lane 1 input.
QSFPDD1_RX_N[2]	Input	230	MGTFRXN1_230	U1	Negative receive lane 2 input.
QSFPDD1_RX_P[2]	Input	230	MGTFRXP1_230	U2	Positive receive lane 2 input.
QSFPDD1_RX_N[3]	Input	230	MGTFRXN2_230	T3	Negative receive lane 3 input.
QSFPDD1_RX_P[3]	Input	230	MGTFRXP2_230	T4	Positive receive lane 3 input.
QSFPDD1_RX_N[4]	Input	230	MGTFRXN3_230	R1	Negative receive lane 4 input.
QSFPDD1_RX_P[4]	Input	230	MGTFRXP3_230	R2	Positive receive lane 4 input.
QSFPDD1_RX_N[5]	Input	231	MGTFRXN0_231	P3	Negative receive lane 5 input.
QSFPDD1_RX_P[5]	Input	231	MGTFRXP0_231	P4	Positive receive lane 5 input.
QSFPDD1_RX_N[6]	Input	231	MGTFRXN1_231	N1	Negative receive lane 6 input.
QSFPDD1_RX_P[6]	Input	231	MGTFRXP1_231	N2	Positive receive lane 6 input.
QSFPDD1_RX_N[7]	Input	231	MGTFRXN2_231	M3	Negative receive lane 7 input.
QSFPDD1_RX_P[7]	Input	231	MGTFRXP2_231	M4	Positive receive lane 7 input.
QSFPDD1_RX_N[8]	Input	231	MGTFRXN3_231	L1	Negative receive lane 8 input.
QSFPDD1_RX_P[8]	Input	231	MGTFRXP3_231	L2	Positive receive lane 8 input.
QSFPDD1_TX_N[1]	Output	230	MGTFTXN0_230	Y8	Negative transmit lane 1 output.
QSFPDD1_TX_P[1]	Output	230	MGTFTXP0_230	Y9	Positive transmit lane 1 output.
QSFPDD1_TX_N[2]	Output	230	MGTFTXN1_230	W6	Negative transmit lane 2 output.
QSFPDD1_TX_P[2]	Output	230	MGTFTXP1_230	W7	Positive transmit lane 2 output.
QSFPDD1_TX_N[3]	Output	230	MGTFTXN2_230	V8	Negative transmit lane 3 output.
QSFPDD1_TX_P[3]	Output	230	MGTFTXP2_230	V9	Positive transmit lane 3 output.
QSFPDD1_TX_N[4]	Output	230	MGTFTXN3_230	U6	Negative transmit lane 4 output.
QSFPDD1_TX_P[4]	Output	230	MGTFTXP3_230	U7	Positive transmit lane 4 output.
QSFPDD1_TX_N[5]	Output	231	MGTFTXN0_231	T8	Negative transmit lane 5 output.
QSFPDD1_TX_P[5]	Output	231	MGTFTXP0_231	T9	Positive transmit lane 5 output.
QSFPDD1_TX_N[6]	Output	231	MGTFTXN1_231	R6	Negative transmit lane 6 output.
QSFPDD1_TX_P[6]	Output	231	MGTFTXP1_231	R7	Positive transmit lane 6 output.
QSFPDD1_TX_N[7]	Output	231	MGTFTXN2_231	P8	Negative transmit lane 7 output.
QSFPDD1_TX_P[7]	Output	231	MGTFTXP2_231	P9	Positive transmit lane 7 output.
QSFPDD1_TX_N[8]	Output	231	MGTFTXN3_231	N6	Negative transmit lane 8 output.
QSFPDD1_TX_P[8]	Output	231	MGTFTXP3_231	N7	Positive transmit lane 8 output.

QSFP-DD2 Interface lane Mapping and High-Speed Connections

Table 9: **QSFP-DD2 Interface lane Mapping**

signal Name	Direction	Bank	I/O Reference	Pin	Description
SYNCE_CLK12_LVDS_N	Input	228	MGTREFCLK0N_228	AE10	REFCLK0 negative LVDS signal.
SYNCE_CLK12_LVDS_P	Input	228	MGTREFCLK0P_228	AE11	REFCLK0 positive LVDS signal.
SYNCE_CLK13_LVDS_N	Input	229	MGTREFCLK0N_229	AA10	REFCLK0 negative LVDS signal.
SYNCE_CLK13_LVDS_P	Input	229	MGTREFCLK0P_229	AA11	REFCLK0 positive LVDS signal.
QSFPDD2_RX_N[1]	Input	228	MGTFRXN0_228	AF3	Negative receive lane 1 input.
QSFPDD2_RX_P[1]	Input	228	MGTFRXP0_228	AF4	Positive receive lane 1 input.
QSFPDD2_RX_N[2]	Input	228	MGTFRXN1_228	AE1	Negative receive lane 2 input.
QSFPDD2_RX_P[2]	Input	228	MGTFRXP1_228	AE2	Positive receive lane 2 input.
QSFPDD2_RX_N[3]	Input	228	MGTFRXN2_228	AD3	Negative receive lane 3 input.
QSFPDD2_RX_P[3]	Input	228	MGTFRXP2_228	AD4	Positive receive lane 3 input.
QSFPDD2_RX_N[4]	Input	228	MGTFRXN3_228	AC1	Negative receive lane 4 input.
QSFPDD2_RX_P[4]	Input	228	MGTFRXP3_228	AC2	Positive receive lane 4 input.
QSFPDD2_RX_N[5]	Input	229	MGTFRXN0_229	AB3	Negative receive lane 5 input.
QSFPDD2_RX_P[5]	Input	229	MGTFRXP0_229	AB4	Positive receive lane 5 input.
QSFPDD2_RX_N[6]	Input	229	MGTFRXN1_229	AA1	Negative receive lane 6 input.
QSFPDD2_RX_P[6]	Input	229	MGTFRXP1_229	AA2	Positive receive lane 6 input.
QSFPDD2_RX_N[7]	Input	229	MGTFRXN2_229	Y3	Negative receive lane 7 input.
QSFPDD2_RX_P[7]	Input	229	MGTFRXP2_229	Y4	Positive receive lane 7 input.
QSFPDD2_RX_N[8]	Input	229	MGTFRXN3_229	W1	Negative receive lane 8 input.
QSFPDD2_RX_P[8]	Input	229	MGTFRXP3_229	W2	Positive receive lane 8 input.
QSFPDD2_TX_N[1]	Output	228	MGTFTXN0_228	AH8	Negative transmit lane 1 output.
QSFPDD2_TX_P[1]	Output	228	MGTFTXP0_228	AH9	Positive transmit lane 1 Output
QSFPDD2_TX_N[2]	Output	228	MGTFTXN1_228	AG6	Negative transmit lane 2 output.
QSFPDD2_TX_P[2]	Output	228	MGTFTXP1_228	AG7	Positive transmit lane 2 output.
QSFPDD2_TX_N[3]	Output	228	MGTFTXN2_228	AF8	Negative transmit lane 3 output.
QSFPDD2_TX_P[3]	Output	228	MGTFTXP2_228	AF9	Positive transmit lane 3 output.
QSFPDD2_TX_N[4]	Output	228	MGTFTXN3_228	AE6	Negative transmit lane 4 output.
QSFPDD2_TX_P[4]	Output	228	MGTFTXP3_228	AE7	Positive transmit lane 4 output.
QSFPDD2_TX_N[5]	Output	229	MGTFTXN0_229	AD8	Negative transmit lane 5 output.
QSFPDD2_TX_P[5]	Output	229	MGTFTXP0_229	AD9	Positive transmit lane 5 output.
QSFPDD2_TX_N[6]	Output	229	MGTFTXN1_229	AC6	Negative transmit lane 6 output.
QSFPDD2_TX_P[6]	Output	229	MGTFTXP1_229	AC7	Positive transmit lane 6 output.
QSFPDD2_TX_N[7]	Output	229	MGTFTXN2_229	AB8	Negative transmit lane 7 output.
QSFPDD2_TX_P[7]	Output	229	MGTFTXP2_229	AB9	Positive transmit lane 7 output.
QSFPDD2_TX_N[8]	Output	229	MGTFTXN3_229	AA6	Negative transmit lane 8 output.
QSFPDD2_TX_P[8]	Output	229	MGTFTXP3_229	AA7	Positive transmit lane 8 output.

QSFP-DD3 Interface lane Mapping and High-Speed Connections

Table 10: **QSFP-DD3 Interface lane Mapping**

Signal Name	Direction	Bank	I/O Reference	Pin	Description
SYNCE_CLK10_LVDS_N	Input	226	MGTREFCLK0N_226	AN10	REFCLK0 negative LVDS signal.
SYNCE_CLK10_LVDS_P	Input	226	MGTREFCLK0P_226	AN11	REFCLK0 positive LVDS signal.
SYNCE_CLK11_LVDS_N	Input	227	MGTREFCLK0N_227	AJ10	REFCLK0 negative LVDS signal.
SYNCE_CLK11_LVDS_P	Input	227	MGTREFCLK0P_227	AJ11	REFCLK0 positive LVDS signal.
QSFPDD3_RX_N[1]	Input	227	MGTFRXN0_227	AK3	Negative receive lane 1 input.
QSFPDD3_RX_P[1]	Input	227	MGTFRXP0_227	AK4	Positive receive lane 1 input.
QSFPDD3_RX_N[2]	Input	227	MGTFRXN1_227	AJ1	Negative receive lane 2 Input
QSFPDD3_RX_P[2]	Input	227	MGTFRXP1_227	AJ2	Positive receive lane 2 input.
QSFPDD3_RX_N[3]	Input	227	MGTFRXN2_227	AH3	Negative receive lane 3 input.
QSFPDD3_RX_P[3]	Input	227	MGTFRXP2_227	AH4	Positive receive lane 3 input.
QSFPDD3_RX_N[4]	Input	227	MGTFRXN3_227	AG1	Negative receive lane 4 input.
QSFPDD3_RX_P[4]	Input	227	MGTFRXP3_227	AG2	Positive receive lane 4 input.
QSFPDD3_RX_N[5]	Input	226	MGTFRXN0_226	AP3	Negative receive lane 5 input.
QSFPDD3_RX_P[5]	Input	226	MGTFRXP0_226	AP4	Positive receive lane 5 input.
QSFPDD3_RX_N[6]	Input	226	MGTFRXN1_226	AN1	Negative receive lane 6 input.
QSFPDD3_RX_P[6]	Input	226	MGTFRXP1_226	AN2	Positive receive lane 6 input.
QSFPDD3_RX_N[7]	Input	226	MGTFRXN2_226	AM3	Negative receive lane 7 input.
QSFPDD3_RX_P[7]	Input	226	MGTFRXP2_226	AM4	Positive receive lane 7 input.
QSFPDD3_RX_N[8]	Input	226	MGTFRXN3_226	AL1	Negative receive lane 8 input.
QSFPDD3_RX_P[8]	Input	226	MGTFRXP3_226	AL2	Positive receive lane 8 input.
QSFPDD3_TX_N[1]	Output	227	MGTFTXN0_227	AM8	Negative transmit lane 1 output.
QSFPDD3_TX_P[1]	Output	227	MGTFTXP0_227	AM9	Positive transmit lane 1 output.
QSFPDD3_TX_N[2]	Output	227	MGTFTXN1_227	AL6	Negative transmit lane 2 output.
QSFPDD3_TX_P[2]	Output	227	MGTFTXP1_227	AL7	Positive transmit lane 2 output.
QSFPDD3_TX_N[3]	Output	227	MGTFTXN2_227	AK8	Negative transmit lane 3 output.
QSFPDD3_TX_P[3]	Output	227	MGTFTXP2_227	AK9	Positive transmit lane 3 output.
QSFPDD3_TX_N[4]	Output	227	MGTFTXN3_227	AJ6	Negative transmit lane 4 output.
QSFPDD3_TX_P[4]	Output	227	MGTFTXP3_227	AJ7	Positive transmit lane 4 output.
QSFPDD3_TX_N[5]	Output	226	MGTFTXN0_226	AT8	Negative transmit lane 5 output.
QSFPDD3_TX_P[5]	Output	226	MGTFTXP0_226	AT9	Positive transmit lane 5 output.
QSFPDD3_TX_N[6]	Output	226	MGTFTXN1_226	AR6	Negative transmit lane 6 output.
QSFPDD3_TX_P[6]	Output	226	MGTFTXP1_226	AR7	Positive transmit lane 6 output.
QSFPDD3_TX_N[7]	Output	226	MGTFTXN2_226	AP8	Negative transmit lane 7 output.
QSFPDD3_TX_P[7]	Output	226	MGTFTXP2_226	AP9	Positive transmit lane 7 output.
QSFPDD3_TX_N[8]	Output	226	MGTFTXN3_226	AN6	Negative transmit lane 8 output.
QSFPDD3_TX_P[8]	Output	226	MGTFTXP3_226	AN7	Positive transmit lane 8 output.

Connectivity Considerations

The following lists considerations for various direct attach copper (DAC) cable usage scenarios.

Table 11: **QSFP-DD Connector Considerations**

	Cable Type	
Consideration	**QSFP-DD**	**QSFP+/QSFP28**
Lanes of connectivity	8 lanes of connectivity span 2 GTF quads.	4 lanes of connectivity to a single GTF quad.
Legacy / DD support	Consists of legacy pins (lanes 1-4) and DD pins (lanes 5-8).	Connects only to the legacy pins (lanes 1-4) of the QSFP-DD connector.
Legacy pin connection	Legacy pins are connected to quads 227, 228, 230, and 232 (QSFP1, 2, 3, 4 respectively)	Connect to quads 227, 228, 230, and 232 (QSFP1, 2, 3, 4 respectively).
DD pin connections	DD pins are connected to quads 226, 229, 231, and 233.	Not connected
Card jitter attenuation support	Provides access to jitter cleanup device via dedicated REFCLK outputs on quads 229 and 231 (QSFP-DD 2 and QSFP-DD 3), or via HPIO (bank 65).	Requires use of HPIO (bank 65) to provide recovered clock to jitter cleanup device (2 outputs available).

Suggested DAC Cables

Any industry standards compliant QSFP+/QSFP28/QSFP-DD DAC cable can be used with the above mentioned considerations. The Amphenol-branded cable is suggested for a QSFP-DD to 8xSFP+ splitter DAC cable.

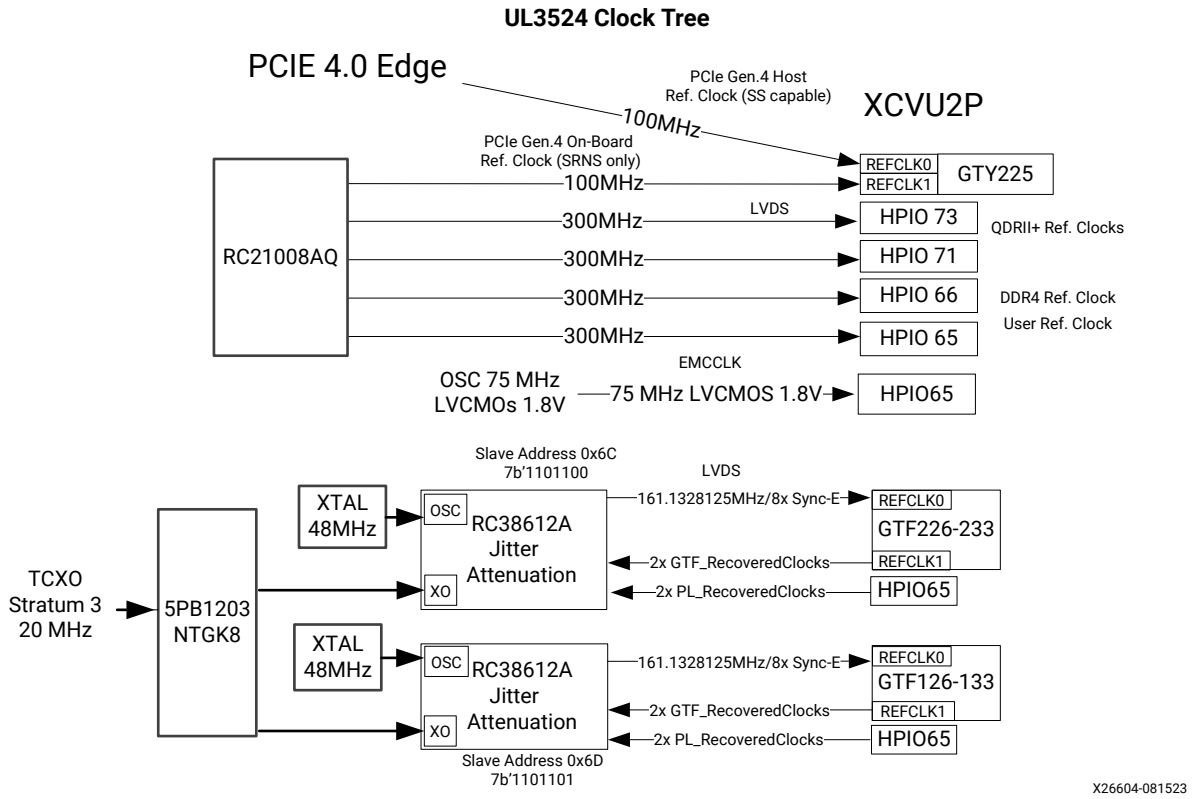
Clocking

The card provides the following reference clocks:

- PCIe® reference clocks
- Memory controller (QDR-II+, DDR4) reference clocks
- User reference clock
- Ethernet reference clocks

The following high-level clock tree diagram shows the advanced clocking and jitter attenuator logic. See the following section for additional details.

Figure 8: **UL3524 Clocking Tree**



The card uses the Renesas RC21008AQ clock generator to provide reference clocks for PCIe, user reference, as well as DDR4 and QDR-II+ memory controllers. The following table lists the Renesas clock output reference and frequency, along with the FPGA destination bank and XDC net names. Renesas clock output references that are not provided in the table are not connected.

Table 12: **Clock Generator Output Frequencies**

Renesas RC21008AQ Clock Output Reference	Frequency	Destination FPGA Bank	Block Reference Clock	XDC Net Name
OUT1	100 MHz	225	PCIe	CLK0_LVDS_100_N CLK0_LVDS_100_P
OUT2	300 MHz	65	User	CLK13_LVDS_300_N CLK13_LVDS_300_P
OUT3	300 MHz	66	DDR4 memory controller	CLK12_LVDS_300_N CLK12_LVDS_300_P
OUT6	300 MHz	71	QDR-II+ memory controller 1	CLK11_LVDS_300_N CLK11_LVDS_300_P
OUT7	300 MHz	73	QDR-II+ memory controller 0	CLK10_LVDS_300_N CLK10_LVDS_300_P

User Clock

A 300 MHz user reference clock is generated by the clock generator and connected directly to FPGA bank 65.

QDR-II+ Memory Controller Clocks

Separate 300 MHz QDR-II+ clocks are generated by the clock generator and connected directly to the following:

- FPGA bank 71 for QDR-II+ memory controller 1.
- FPGA bank 73 for QDR-II+ memory controller 0.

DDR4 Memory Controller Clock

A 300 MHz DDR4 reference clock is generated by the clock generator and connected directly to FPGA bank 67.

PCIe Reference Clocks

The following two clocks are provided to support PCIe clocking.

Table 13: **PCIe Reference Clocks**

Clock Source	Description
PCIe Edge Connector	100 MHz clock originating from the PCIe edge connector and connected to GTY 225 MGTREFCLK0 inputs. The clock signal is AC coupled.
Internal clock generator	100 MHz clock originating from the Renesas RC21008AQ clock generator and connected to GTY 225 MGTREFCLK1 inputs. The clock signal is AC coupled and meets PCIe Gen3/Gen4 jitter specifications.

FPGA EMCCLK Programming Clock

To minimize clock startup time, a 75 MHz FPGA external master configuration clock (EMCCLK) is sourced from an onboard oscillator. It is connected directly to the dedicated (EMCCLK), on bank 65.

Ethernet Reference Clocks

A 161.1328125 MHz Ethernet reference clock is generated.

Jitter Attenuator

There are two jitter attenuator (cleaner) blocks which support the following two GTF groups:

- Jitter Cleaner 1: Banks 226-233 for QSFP-DD ports.
- Jitter Cleaner 2: Banks 126-133 for ARF6 expansion ports.

The logic for each block is identical and consists of various temperature-controlled crystal oscillators and ultra-low jitter components that provide exceptional jitter attenuation and clock fidelity.

The major components of the jitter attenuator block are given in the following table.

Table 14: **Jitter Attenuation Components**

Part	Use
CTS Stratum 3 TCXO Oscillators	Oscillator
Renesas 5PB1203	Clock fanout buffer
Renesas RC38612	Jitter cleaner (synchronizer) to regenerate and distribute ultra-low jitter clock locked to IEEE 1588.

The Resesas jitter cleaner device (RC38612) is the heart of the jitter attenuation logic. It has the ability to load a number of programming configurations and the flexibility to route input clocks through an array of internal Digitally Controlled Oscillator (DCO) or Digital Phase LockLoop (DPLL) before routing to the output clocks. Designers should closely examine the Renesas user guide to fully understand how to configure and use the device.

The following figure shows the high-level connections between the QSFP-DD and ARF6 expansion port GTFs, and their respective Renesas jitter cleaners. Each jitter cleaner can select one of four recovered clock inputs. The four recovered clocks are split into these two groups:

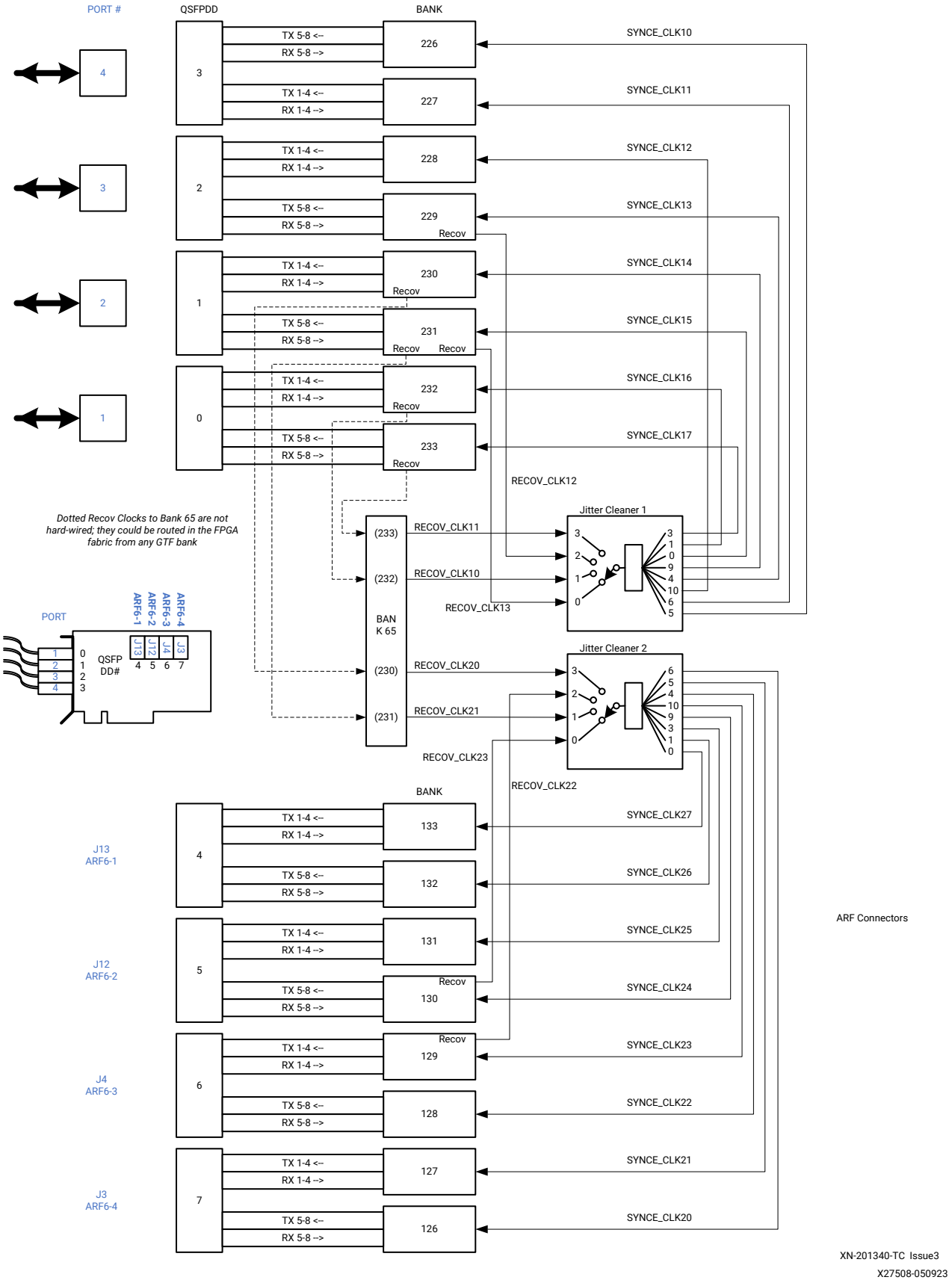
- Two recovered clocks come directly from dedicated GTFs
- Two recovered clocks are indirectly routed from the GTF via FPGA bank 65

In addition, each jitter cleaner produces eight attenuated outputs. While the jitter cleaner has some flexibility in connection of outputs to internal DCO/DPLLs, it does not allow all eight outputs to be connected to the same DPLL.

The PLL can be steered over I2C bus to align Sync-E clock phase with internal FPGA precision time point reference clock. Sync-E outputs can be flexibly assigned to PLLs creating Sync-E subgroups. Sync-E reference clocks are connected to MGTREFCLK0 of every quad belonging to the group.

IMPORTANT! *The four external recovery clocks from banks 129 (`RECOV_CLK22`), 130 (`RECOV_CLK23`), 229 (`RECOV_CLK12`), and 231 (`RECOV_CLK13`) are hardwired to the jitter cleaners. The four recovery clocks (`RECOV_CLK10`, `RECOV_CLK11`, `RECOV_CLK20`, and `RECOV_CLK21`) are internally routed through bank 65 and can be sourced from any of the GTF banks through the FPGA fabric. In the following figure, the dashed lines represent only one example configuration for recovery clocks from banks 230, 231, 232, and 233.*

Figure 9: **QSFP-DD and Expansion Port Jitter Attenuation Connections**



Renesas Recovered Clock FPGA Bank Source and Associated XDC Net Name

The following two tables provide the FPGA bank source and associated XDC net name of the signals connected to the clock inputs of the QSFP-DD and ARF6 expansion port Renesas jitter cleaners, respectively. See the UL3524 XDC file.

Table 15: **QSFP-DD to Jitter Attenuator Recovered Clock Connection**

Renesas Recovered Clock Reference	Source BANK	FPGA Pin	XDC Net Name
CLK0	231	J10	RECOV_CLK13_LVDS_P
		J11	RECOV_CLK13_LVDS_N
CLK1	65[2]	BE18	RECOV_CLK10_LVDS_P
		BF18	RECOV_CLK10_LVDS_N
CLK2	229	W10	RECOV_CLK12_LVDS_P
		W11	RECOV_CLK12_LVDS_N
CLK3	65[2]	BF20	RECOV_CLK11_LVDS_P
		BF19	RECOV_CLK11_LVDS_N
CLK4	NC[1]		

Notes:

1. *NC* indicates no connection to the port.
2. The four recovery clocks (RECOV_CLK10, RECOV_CLK11, RECOV_CLK20, and RECOV_CLK21) are internally routed through bank 65 and thus can be sourced from any of the GTF banks through the FPGA fabric.

Table 16: **ARF6 Expansion Port to Jitter Attenuator Recovered Clock Connection**

Renesas Recovered Clock Reference	BANK	FPGA Pin	XDC Net Name
CLK0	130	N36	RECOV_CLK23_LVDS_P
		N37	RECOV_CLK23_LVDS_N
CLK1	65[2]	BA20	RECOV_CLK21_LVDS_P
		BB20	RECOV_CLK21_LVDS_N
CLK2	129	U36	RECOV_CLK22_LVDS_P
		U37	RECOV_CLK22_LVDS_N
CLK3	65[2]	BC19	RECOV_CLK20_LVDS_P
		BD19	RECOV_CLK20_LVDS_N
CLK4	NC[1]		

Notes:

1. *NC* indicates no connection to the port.
2. The four recovery clocks (RECOV_CLK10, RECOV_CLK11, RECOV_CLK20, and RECOV_CLK21) are internally routed through bank 65 and thus can be sourced from any of the GTF banks through the FPGA fabric.

FPGA Bank Destination and Associated XDC Net Name

The following two tables provide the FPGA bank destination and associated XDC net name of the signals connected to the SYNC-E clock outputs for QSFP-DD and ARF6 expansion port Renesas jitter cleaners respectively. See the UL3524 XDC file.

Table 17: **Jitter Attenuator to QSFP-DD SYNC-E Clock Connection**

Renesas Output Clock Reference	BANK	FPGA Pin	XDC Net Name
Q0	231	N11	SYNCE_CLK15_LVDS_P
		N10	SYNCE_CLK15_LVDS_N
Q1	232	H9	SYNCE_CLK16_LVDS_P
		H8	SYNCE_CLK16_LVDS_N
Q2	NC[1]		
Q3	233	D9	SYNCE_CLK17_LVDS_P
		D8	SYNCE_CLK17_LVDS_N
Q4	229	AA11	SYNCE_CLK13_LVDS_P
		AA10	SYNCE_CLK13_LVDS_N
Q5	226	AN11	SYNCE_CLK10_LVDS_P
		AN10	SYNCE_CLK10_LVDS_N
Q6	227	AJ11	SYNCE_CLK11_LVDS_P
		AJ10	SYNCE_CLK11_LVDS_N
Q7	NC[1]		
Q8			
Q9	230	U11	SYNCE_CLK14_LVDS_P
		U10	SYNCE_CLK14_LVDS_N
Q10	228	AE11	SYNCE_CLK12_LVDS_P
		AE10	SYNCE_CLK12_LVDS_N
Q11	NC[1]		

Notes:

1. *NC* indicates no connection to the port.

Table 18: **Jitter Attenuator to ARF6 Expansion Port SYNC-E Clock Connection**

Renesas Output Clock Reference	BANK	FPGA Pin	XDC Net Name
Q0	133	D38	SYNCE_CLK27_LVDS_P
		D39	SYNCE_CLK27_LVDS_N
Q1	132	H38	SYNCE_CLK26_LVDS_P
		H39	SYNCE_CLK26_LVDS_N
Q2	NC[1]		
Q3	131	L36	SYNCE_CLK25_LVDS_P
		L37	SYNCE_CLK25_LVDS_N
Q4	128	AC36	SYNCE_CLK22_LVDS_P
		AC37	SYNCE_CLK22_LVDS_N

Table 18: **Jitter Attenuator to ARF6 Expansion Port SYNC-E Clock Connection** *(cont'd)*

Renesas Output Clock Reference	BANK	FPGA Pin	XDC Net Name
Q5	127	AG36	SYNCE_CLK21_LVDS_P
		AG37	SYNCE_CLK21_LVDS_N
Q6	126	AL36	SYNCE_CLK20_LVDS_P
		AL37	SYNCE_CLK20_LVDS_N
Q7	NC[1]		
Q8			
Q9	130	R36	SYNCE_CLK24_LVDS_P
		R37	SYNCE_CLK24_LVDS_N
Q10	129	W36	SYNCE_CLK23_LVDS_P
		W37	SYNCE_CLK23_LVDS_N
Q11	NC[1]		

Notes:

1. *NC* indicates no connection to the port.

Renesas Default and Predefined Configuration Settings

Both Renesas RC38612A devices used on the UL3524 card have an identical internal one-time programmable (OTP) memory with four predefined configuration register settings (configuration 12 through 15). Configuration 15 is the default setting and is loaded on power-up or device reset.

The configuration register settings represent the default values that the Renesas device registers take on power-up or reset. These register values can be changed after power-up or reset via the serial port. Any changes are lost when the device is reset or power-cycled unless programmed into OTP as an additional or replacement configuration.

The values on ports GPIO[3:0] (ports JITT1_GPOI0 - JITT1_GPOI3 for Jitter Cleaner 1 and ports JITT2_GPOI0 - JITT2_GPOI3 for Jitter Cleaner 2) are used to select the initial configuration from the OTP memory. The following table shows the configuration selection as a function of GPIO[3:0].

Table 19: **Jitter Cleaner Configuration Selection**

GPIO[3:0]	Configuration Selection
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	10

Table 19: **Jitter Cleaner Configuration Selection** *(cont'd)*

GPIO[3:0]	Configuration Selection
1011	11
1100	12
1101	13
1110	14
1111	15

The UL3524 card has GPIO[3:0] pulled high (4'b1111). Consequently, when powered on configuration 15 is selected as the default configuration. The following tables show the DPLL source and frequency output for configurations 12 through 15. The default configuration applies equally to both the QSFP-DD and expansion port jitter attenuators.

Table 20: **Renesas Configuration Setting 12**

Source	Output	Frequency (MHz)
DPLL0	OUT0	156.25
DPLL0	OUT1	156.25
DNone	OUT2	OFF
DPLL1	OUT3	156.25
DPLL1	OUT4	156.25
DPLL2	OUT5	156.25
DPLL3	OUT6	156.25
DNone	OUT7	OFF
DNone	OUT8	OFF
DPLL5	OUT9	156.25
DPLL5	OUT10	156.25
DNone	OUT11	OFF

Table 21: **Renesas Configuration Setting 13**

Source	Output	Frequency (MHz)
DPLL0	OUT0	161.1328125
DPLL0	OUT1	161.1328125
DNone	OUT2	OFF
DPLL1	OUT3	161.1328125
DPLL1	OUT4	161.1328125
DPLL3	OUT5	161.1328125
DPLL3	OUT6	161.1328125
DNone	OUT7	OFF
DNone	OUT8	OFF
DPLL5	OUT9	161.1328125
DPLL5	OUT10	161.1328125
DNone	OUT11	OFF

Table 22: **Renesas Configuration Setting 14**

Source	Output	Frequency (MHz)
DPLL0	OUT0	156.25
DPLL0	OUT1	156.25
DNone	OUT2	OFF
DPLL0	OUT3	156.25
DPLL0	OUT4	156.25
DPLL0	OUT5	156.25
DPLL3	OUT6	156.25
DNone	OUT7	OFF
DNone	OUT8	OFF
DPLL0	OUT9	156.25
DPLL0	OUT10	156.25
DNone	OUT11	OFF

Table 23: **Renesas Configuration Setting 15 (Default Configuration)**

Source	Output	Frequency (MHz)
DPLL0	OUT0	161.1328125
DPLL0	OUT1	161.1328125
DNone	OUT2	OFF
DPLL0	OUT3	161.1328125
DPLL0	OUT4	161.1328125
DPLL0	OUT5	161.1328125
DPLL3	OUT6	161.1328125
DNone	OUT7	OFF
DNone	OUT8	OFF
DPLL0	OUT9	161.1328125
DPLL0	OUT10	161.1328125
DNone	OUT11	OFF

Renesas Reset Sequence

During its reset sequence, the RC38612 jitter cleaner will:

- Load its initial configuration.
- Enable internal regulators.
- Establish and enable internal clocks.
- Perform initial calibration of the Analog PLL.
- Lock it to the reference on the OSCI/OSCO pins.

For complete details, see the RC38612 datasheet.

Loading a Configuration

For complete details on how to load a configuration, see the RC38612 datasheet. The following details the high-level steps to load a configuration.

1. Set the required CONFIG Value on JITT1_GPIO0-GPIO3 (for example, Config 15 – 1111 Config 14 – 1110).
2. Assert JITT_RESETn to logic 0 (resets the RC38612 devices).
3. Give some delay (> 10 ms).
4. Assert JITT_RESETn to logic 1 (gets the RC38612 devices out of reset).
5. Monitor JITT1_GPIO5 – when it is asserted to logic 1 it indicates that the TX clocks generated by the RC38612 devices are in sync with the recovered clock.

Satellite Controller

The satellite controller (SC) provides independent supervisory and card management functions including power and temperature monitoring. The host server board management controller (BMC) can interact with the satellite controller to monitor and control the card through out-of-band (OOB) communication.

Note: Power to the SC is dependent on the power mode selected. See Power Modes of Operation.

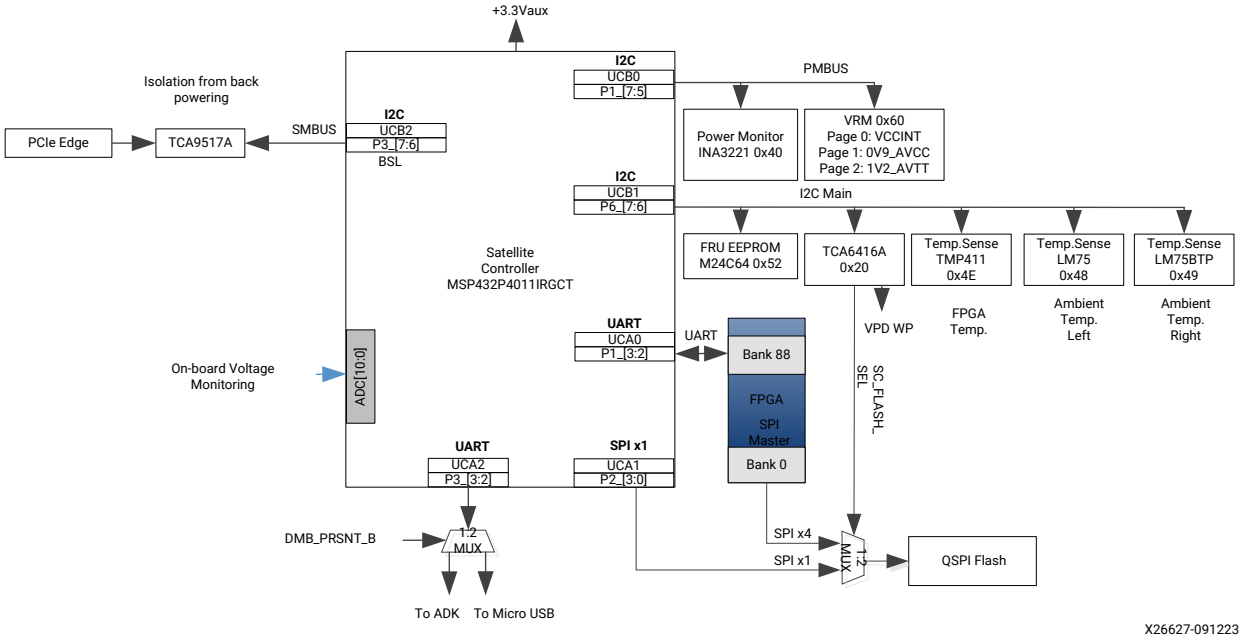
The following table details the SC component used.

Table 24: **Satellite Controller Device Details**

Parameter	Description
Manufacturer	TI
Part number	MSP432P4011IRGCT
Details	Low power MCU

The following figure shows the interfaces and devices that are accessible by the SC.

Figure 10: **Satellite Controller Interface and Device Access**



Out-of-Band Support

The Alveo Card Out-of-Band Management Specification for Server BMC documentation describes out-of-band (OoB) support implemented in the SC firmware, supporting communication with the server board management controller (BMC) over the SMBus/I2C interface on the PCIe edge connector. The underlying protocols supported are standard I2C protocol and PLDM over MCTP over SMBus.

The *Card Management Solution Subsystem Product Guide* (PG348) provides card management solution IP allowing you to quickly develop and interact with the satellite controller from the FPGA.

Satellite Firmware Update

To update the SC firmware, you must generate an AMD Vivado™ design that implements the CMS IP. See reference designs for support details.

Satellite Sensor Data Access

The SC has access to the following temperature sensors. See *System I2C_MAIN_SCL / SDA* and *Power PMBUS_SCL / SDA* in I2C Register Map, for register details.

- FPGA temperature sensor
- Card inlet and outlet temperature sensors

To read the SC sensor information, a design using the CMS IP (see reference designs for support details) and host application to communicate with the CMS IP is required.

Card Thermal and Electrical Protections

Built-in shutdown logic protects the card from damage by removing power to the FPGA when either electrical or thermal limits (given in the following table) reach or exceed their respective card shutdown thresholds. VCCINT current and temperature are monitored by the card regulator while FPGA temperature is monitored by the satellite controller (SC). Power to the card SC remains on during card shutdown. Card shutdown protection logic is always enabled and cannot be disabled.

***Note*:** When card shutdown occurs, the card is pulled off the PCIe bus and consequently is not seen by the host. No AXI firewall trip is issued. A cold reboot of the server is required to recover.

The following table lists the card shutdown power and thermal thresholds.

Table 25: **Thermal and Electrical Protection Thresholds**

Sensor Description	Card Shutdown Threshold
VCCINT Current	65A per phase, total two phase (65 x 2 = 130A)
VCCINT Temperature	125°C
FPGA Temperature	107°C

PPS In

One PPS (one pulse per second) input interface, located on the PCIe I/O bracket, provides synchronization between external system clock synchronization units. The 1PPS input interface is compatible with plug-type SSMB adaptors and cables (such as Pasternack PE3139LF series cables) and is terminated with a 50Ω load. The following table provides the XDC net name and associated pin assignment.

Table 26: **PPS Pin Assignment**

Net Name	Pin Assignment
PPS_IN_FPGA	BF14

PCIe AUX Power

The card has an 8-pin PCIe auxiliary power connector. A PCIe auxiliary power cable must be plugged into the connector for the card to operate correctly.

Depending on your server or computer, an additional PCI Express auxiliary power cable or adapter might be needed. Consult your computer documentation for additional information.

***Note*:** This 8-pin connector is not compatible with an ATX12V/EPS12V power cable source. Ensure that the appropriate PCIe auxiliary power source is available, not an ATX12V/EPS12V power source. For more details see Answer Record 72298.

For card installation and connecting the PCIe AUX power cable, see the *Alveo UL3524 Installation Guide* (UG1584).

DDR4 Specifications

There is a total of 16 GB DDR4 memory on the UL3524 card comprising nine x8 Micron components. The following table details the DDR4 memory component used.

Table 27: **DDR4 Component Specification**

Parameter	Description
Manufacturer	Micron
Part number	MT40A2G8SA-062E
Total number parts on card	8 + 1
Details	• 16 Gb DDR4 (16 GB total on the card) • Single rank • Supports ECC error detection and corrections • Supports 64b + 8b ECC at 2666 MT/s

***Note*:** The DDR4 memory subsystem has a separate power control from FPGA and must be enabled prior to use. See reference designs for support details.

QDR II+ Specifications

There are two QDR II+ x18 memory components on the card for a total of 72 MB (2 x 288 Mb) of memory. Each operates at 550 MHz at 1.5V I/O Voltage. The following table details the QDR II+ memory component.

Table 28: **QDR II+ Component Specification**

Parameter	Description
Manufacturer	GSI Technology
Part number	GS82582DT20GE-550
Details	• Speed: 550 MHz • Density: 288 Mb • Configuration: x18

Each QDR-II+ controller is implemented in a separate HPIO duplet.

Expansion Ports

The expansion ports provide capabilities to add additional four QSFP-DD connections and sideband control. These ports consist of the following:

- Four high-speed SAMTEC ARF6-16-S-D-A connectors (see https://www.samtec.com/) providing 32 expansion GTF TX/RX pairs over cable using the SAMTEC ARF6 solution.
- Two PicoClasp 10-pin connectors for sideband signals (Molex 5044491007 part).
- The TX lanes are AC coupled, which allows multiple cards to be interconnected.

GTF to Expansion Connector Lane Mapping

The GTF to expansion connector lane mapping and high-speed connection details can be found in the UL3524 XDC file.

Expansion Sideband Connector

Two vertical 10-pin PicoClasp connectors provide sideband access. The following table lists the ARF6 I2C details along with the respective reset per ARF6. The signals on connectors sideband 1 and 2 are physically connected.

Table 29: **Sideband Connector to FPGA Pinout**

Port Name	FPGA Pin	Sideband Connector Pin	Description
ARF_I2C_SCL	M14	6	Expansion port I2C interface.
ARF_I2C_SDA	M13	5	Expansion port I2C interface.
ARF_IO0_RST	K15	3	Expansion port ARF6-0 reset.
ARF_IO1_RST	L15	4	Expansion port ARF6-1 reset.
ARF_IO2_RST	H14	9	Expansion port ARF6-2 reset.
ARF_IO3_RST	H13	2	Expansion port ARF6-3 reset.
ARF_MUX_INTN	L13	8	MUXed expansion port interrupt.
ARF_MUX_RESET	K16	7	MUX expansion port reset.
3.3V		1	Power
GND		10	Ground

***Note*:** The RX polarity of the GTs need to be inverted on the ARF connector when using a loopback cable.

FPGA Configuration Memory

The card is populated with 2 Gb QSPI flash memory, which provides space to store up to four maximum-sized FPGA bitstreams. The following table details the QSPI component.

Table 30: **QSPI Device Details**

Parameter	Description
Manufacturer	Micron
Part number	MT25QU02GCBB8E12
Details	Speed 75 MHz Density 2 Gb (256M x 8)

Two FPGA configuration modes are supported:

- Master SPI x4
- JTAG (over Micro-USB or ADK2 debug connector)

The FPGA bank 0 mode pins are hardwired to master SPI mode M[2:0] = 001 with pull-up/pull-down resistors. At power up, the FPGA is configured by the Quad SPI NOR flash device using the primary serial configuration mode.

Table 31: **Configuration Modes**

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master SPI	001	x1, x2, x4	FPGA output
JTAG	Not applicable – JTAG overrides	x1	Not applicable

Maintenance Interfaces

The card comes with two maintenance interfaces:

- micro USB (two ports available: micro USB0 and micro USB1)
- ADK2 debug connector

Each is described in more detail in subsequent sections. The following table shows the protocols supported for each interface.

Table 32: **ADK2 Debug Connector and micro USB Supported Protocols**

Protocol	micro USB	ADK2
FPGA JTAG	YES	YES
FPGA UART0	YES	NO
FPGA UART1	YES	YES
MSP debug UART	YES	YES
MSP JTAG	NO	YES
SMBus	NO	YES
PMBus	NO	YES

***Note*:** Internal logic is shared between the interfaces. For selecting an interface, refer to ADK2 & USB Port Precedence.

Micro-USB Interface

The card has two micro USB interfaces. Both provide access to the FPGA JTAG/UART +SC UART.

- **micro USB0:** Located on the I/O bracket and accessible outside the chassis.

  micro USB0 might be partially covered by the server chassis, which can make it difficult to plug into.

- **micro USB1:** Located within the retainer bracket and accessible within the chassis.

For their locations, see Card Interfaces.

For accessing the ADK2 or USB interface, along with details on precedence on USB selection, see ADK2 & USB Port Precedence.

ADK2 Debug Connector

The ADK2 debug connector, with the AMD Alveo™ debug kit (ADK), provides communication between the card and a host computer or an off-the-shelf debugger. It provides access to the on-board sensors, satellite controller, and QSPI flash programming. For setup details, see *Alveo Card Debug Kit User Guide* (UG1538).

ADK2 Debug Connector Pinout

The following table lists the ADK2 debug connector pin signals for the UL3524.

Note: Both *SC* and *SUC* are synonymous with Satellite Controller.

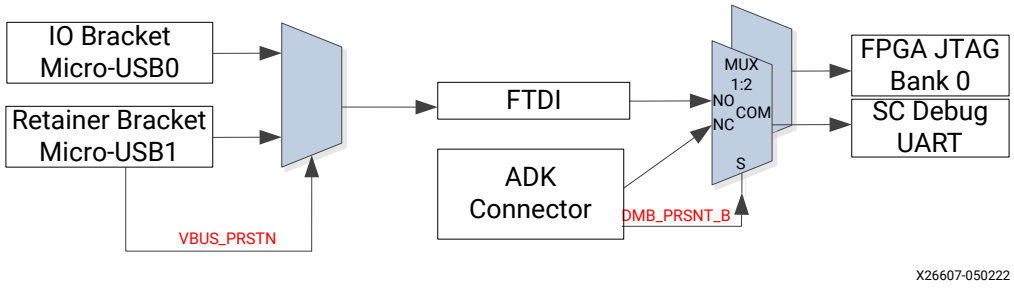
Table 33: **ADK2 Debug Connector Pinout Signals for UL3524**

Pin	Description	Pin	Description
A1	QDR_JTAG_VREF (+1V5_SYS)	B1	FPGA_JTAG_VREF (+3V3_SYS)
A2	QDR_JTAG_TDI	B2	FPGA _JTAG_TCK
A3	QDR_JTAG_TMS	B3	FPGA _JTAG_TMS
A4	QDR_JTAG_TCK	B4	FPGA _JTAG_TDI
A5	QDR_JTAG_TDO	B5	FPGA _JTAG_TDO
A6		B6	NoConnect
A7	NoConnect	B7	
A8	GND	B8	GND
A9		B9	+3V3_SYS_FPGA
A10		B10	FPGA_UART1_RXD
A11		B11	FPGA_UART1_TXD
A12	GND	B12	NoConnect
A13	ALL_PSU_ON_R	B13	SUC_ DEBUG _RXD
A14	SUC_JTAG_TCK	B14	SUC_ DEBUG _TXD
A15		B15	
A16	SUC_JTAG_TDI	B16	
A17	SUC_JTAG_TMS	B17	
A18	SUC_JTAG_TDO	B18	NoConnect
A19	FPGA_MODE_CNTRL	B19	NoConnect
A20		B20	+3V3_AUX
A21	PMBus_SDA	B21	SMBUS_SDA
A22	PMBus_SCL	B22	SMBUS_SCL
A23	PMBus_ALERTB	B23	NoConnect
A24	GND	B24	GND
A25	DDR4_VPP, divided 1:2 divided 2:5	B25	VCCINT (0.9V)
A26	+3V3_SYS_AUX, divided 1:2	B26	+1V8_MGT VCCAUX
A27	5V0, divided 1:5	B27	0V9_MGTAVCC
A28	1V8_SYS	B28	1V2_MGTAVTT
A29	1V5_SYS	B29	1V2_VCCO
A30	DMB_PRSNT_B	B30	GND

ADK2 & USB Port Precedence

The ADK2 and micro USB UART and JTAG interfaces share internal logic to access the various protocols. The following figure shows the shared internal logic with muxing control signals VBUS_PRSTN and DMB_PRSNT_B. These signals are internally set when either micro USB or ADK2 cables are plugged in, respectively.

Figure 11: **USB and ADK2 Debug Connector Mixing**



Access control is granted based on the following precedence rules:

- If the ADK2 debug module is connected, it has control of the shared ports.
- If ADK2 is not connected, USB has control of the shared ports.
  - If connected, micro USB1 has control,
  - If not, micro USB0 has control.

Mechanical

The UL3524 card dimensions, shown in the following table, are compliant with PCIe CEM rev.4.0 full height, ¾ length card specifications.

Table 34: **Card Dimensions**

Parameter	Dimension
Height	111.15 mm
Primary side width	14.47 mm Max
Secondary side width	2.67 mm Max
Length	254 mm
Weight	832g

Thermal

Operating and Storage Temperature Conditions

The following table provides the operating and storage temperatures, and humidity conditions.

Table 35: **Operating and Storage Temperatures and Humidity Conditions**

Specification	Condition
Operating temperature	0°C to 45°C
Storage temperature	–40°C to 75°C
Operating humidity, non-condensing	8% to 90%, and a dew point of –12°C
Storage humidity, non-condensing	5% to 95%

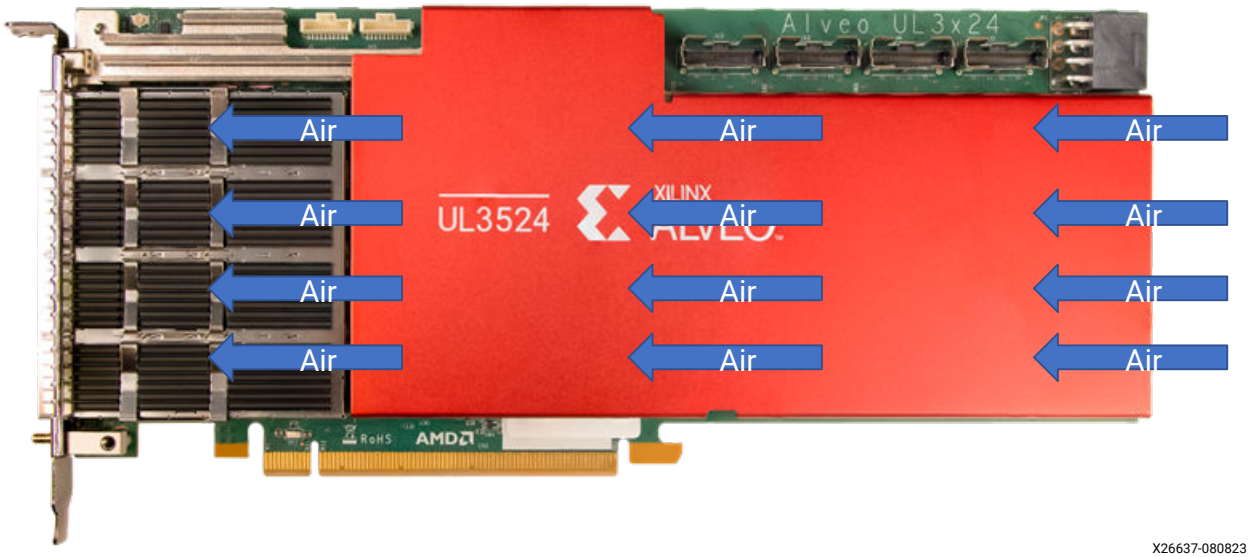
Notes:

1. Refer to Airflow Requirements for operating temperatures and their corresponding airflow and airspeed.

Airflow Direction Support

The UL3524 card is designed for passive cooling and requires an external mechanism to ensure proper airflow for cooling. The card supports normal (forward) airflow direction from retainer bracket to I/O bracket, as illustrated in the following figure. Passive cards should not be powered without a forced airflow mechanism in place.

Figure 12: **Supported Airflow Directions for UL3524 Card**



Note: Other environmental conditions are possible, including bidirectional flow. However, this is specific to server configurations, and testing is performed by individual OEMs. Contact your server provider for more information and options.

Airflow Requirements

Inlet temperature versus airflow requirement in server are given in the following tables.

Note: The thermal characterization results presented in the following tables were obtained using a Dell R740 server. The card was installed in slot 8, riser 3. This is the only slot which provides the required airflow performance on the Dell R740 server. Slot and riser locations for the Dell R740 server are provided in the *Dell EMC PowerEdge R740 Installation and Service Manual*.

Table 36: **UL3524 Inlet Temperature vs. Airflow (out of I/O Bracket) Requirement of PCIe Card Slot (98.4 mm x 20.33 mm) at Sea Level for 125W Total Card Power**

Inlet Temperature to the Card (°C)	With QSFP (3.5W) Rated at 85°C				With QSFP (7.0W) at 85°C			
	CFM	R740 PWM (%)	LFM	Static Pressure (inwg)	CFM	R740 PWM (%)	LFM	Static Pressure (inwg)
25	6.2	-	286	0.24	8.4	~50	391	0.46
30	7.1	~35	328	0.31	10.3	~75	478	0.63
35	8.3	~50	385	0.40	12.9	~100	599	0.90
40	10.0	~75	463	0.56	16.6	-	773	1.36
45	12.4	~100	577	0.83	22.3	-	1034	2.24

Table 37: **UL3524 Inlet Temperature vs. Airflow (out of I/O Bracket) Requirement of PCIe Card Slot (98.4 mm x 20.33 mm) at 1200m above Sea Level for 125W Total Card Power**

Inlet Temperature to the Card (°C)	With QSFP (3.5W) Rated at 85°C				With QSFP (7.0W) Rated at 85° C			
	CFM	R740 PWM (%)	LFM	Static Pressure (inwg)	CFM	R740 PWM (%)	LFM	Static Pressure (inwg)
25	6.8	~35	318	0.29	9.4	~75	435	0.50
30	7.9	~50	366	0.37	11.5	~100	534	0.72
35	9.3	~75	430	0.49	14.4	-	670	1.09
40	11.2	~100	518	0.68	18.6	-	865	1.75
45	14.0	-	648	1.02	25.0	-	1160	3.03

Regulatory Compliance Statements

FCC Class A Products

***Note*:** These devices are for use with UL Listed Servers or I.T.E.

Safety Compliance

The following safety standards apply to all products listed above.

- EU LVD Directive 2014/35/EU
- IEC 62368-1:2020/A11:2020

EMC Compliance

The following standards apply.

Class A Products

- FCC Part 15 – Radiated & Conducted Emissions (USA)
- CAN ICES-3(A)/NMB-3(A) – Radiated & Conducted Emissions (Canada)

- CISPR 32 – Radiated & Conducted Emissions (International)
- EN55032: 2015 – Radiated & Conducted Emissions (European Union)
- EN55035:2017 – Immunity (European Union)
- EMC Directive 2014/30/EU
- Electromagnetic Compatibility Regulations 2016 (UK)
- VCCI (Class A)– Radiated & Conducted Emissions (Japan)
- CNS13438 – Radiated & Conducted Emissions (Taiwan)
- CNS15936, C6459
- CNS 15663 - RoHS (Taiwan)
- AS/NZS CISPR 32 – Radiated and Conducted Emissions (Australia/New Zealand)
- Article 58-2 of Radio Waves Act, Clause 3 (Korea)

Regulatory Compliance Markings

When required, these products are provided with the following Product Certification Markings:

- UL Listed Accessories Mark for the USA and Canada
- CE mark
- UKCA mark
- FCC markings
- VCCI marking
- Australian C-Tick mark
- Korea MSIP mark
- Taiwan BSMI mark

FCC Class A User Information

The Class A products listed above comply with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

IMPORTANT! *This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his or her own expense.*

IMPORTANT! *Cet équipement a été testé et jugé conforme à la Class A digital device, conformément à la règle 15 du standard FCC. Ces limites sont conçues pour fournir des protections contre des interférences nuisibles lorsque l'équipement est utilisé dans un environnement commercial. Cet équipement génère, utilise et peut émettre des énergies de radio-fréquence et, s'il n'est pas installé et utilisé conformément aux instructions, peut nuire aux communications radio. L'exploitation de cet équipement dans une zone résidentielle est susceptible de causer des interférences nuisibles, auquel cas l'utilisateur peut être tenu de prendre des mesures adéquates à ses propres frais.*

WICHTIG! *Dieses Gerät wurde getestet und entspricht den Grenzwerten für digitale Geräte der Klasse A gemäß Teil 15 der FCC-Bestimmungen. Diese Grenzwerte bieten einen angemessenen Schutz gegen schädliche Interferenzen, wenn das Gerät in einer gewerblichen Umgebung betrieben wird. Dieses Gerät erzeugt und verwendet Hochfrequenzenergie und kann diese abstrahlen. Wenn es nicht gemäß den Anweisungen installiert und verwendet wird, kann dies Funkstörungen verursachen. Der Betrieb dieses Geräts in einem Wohngebiet kann schädliche Interferenzen verursachen. In diesem Fall muss der Benutzer die Interferenz auf eigene Kosten beheben.*

CAUTION! *If the device is changed or modified without permission from AMD, the user may void his or her authority to operate the equipment.*

ATTENTION! *Si l'appareil est modifié sans l'autorisation de AMD, l'utilisateur peut annuler son abilité à utiliser l'équipement.*

VORSICHT! *Wenn das Gerät ohne Erlaubnis von AMD geändert wird, kann der Benutzer seine Berechtigung zum Betrieb des Geräts verlieren.*

Canadian Compliance (Industry Canada)

CAN ICES-3(A)/NMB-3(A)

China RoHS Compliance

- SJ/T 11363-2006, 11364-2006, and GB/T 26572-2011
- RoHS 3 directive 2015/863
- EU 2015/863

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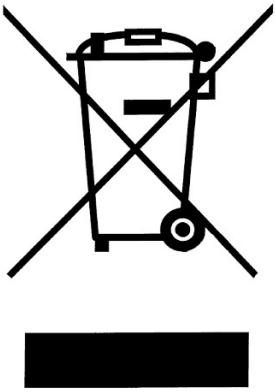

Manufacturer Declaration European Community

CE

Manufacturer Declaration

AMD declares that the equipment described in this document is in conformance with the requirements of the European Council Directive listed below:

- Low Voltage Directive 2014/35/EU
- EMC Directive 2014/30/EU

These products follow the provisions of the European Directive 2014/53/EU.

Dette produkt er i overensstemmelse med det europæiske direktiv 2014/53/EU.

Dit product is in navolging van de bepalingen van Europees Directief 2014/53/EU.

Tämä tuote noudattaa EU-direktiivin 2014/53/EU määräyksiä.

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Dieses Produkt entspricht den Bestimmungen der Europäischen Richtlinie 2014/53/EU.

Þessi vara stenst reglugerð Evrópska Efnahags Bandalagsins númer 2014/53/EU.

Questo prodotto è conforme alla Direttiva Europea 2014/53/EU.

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Este produto cumpre com as normas da Diretiva Européia 2014/53/EU.

Este producto cumple con las normas del Directivo Europeo 2014/53/EU.

Denna produkt har tillverkats i enlighet med EG-direktiv 2014/53/EU.

This declaration is based upon compliance of the Class A products listed above to the following standards:

EN 55032 (CISPR 32 Class A) RF Emissions Control.
EN 55024:2010 (CISPR 24) Immunity to Electromagnetic Disturbance.
EN 50581:2012 - Technical documentation for the assessment of electrical and electronic products with respect to the restriction of hazardous substances.

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ATTENTION! *Dans un environnement domestique, les produits de Classe A peuvent causer des interférences radio, auquel cas l'utilisateur peut être tenu de prendre des mesures adéquates.*

VORSICHT! *In einer häuslichen Umgebung können Produkte der Klasse A Funkstörungen verursachen. In diesem Fall muss der Benutzer möglicherweise geeignete Maßnahmen ergreifen.*

Responsible Party

AMD, Inc.
2100 Logic Drive, San Jose, CA 95124
United States of America
Phone: (408) 559-7778

References

These documents provide supplemental material useful with this data sheet:

1. *Card Management Solution Subsystem Product Guide* (PG348)
2. *Alveo Debug Kit User Guide* (UG1538)
3. UL3524 XDC File
4. UL3524 Master Answer Record
5. *Renesas RC36812 datasheet* https://www.renesas.com/us/en/document/dst/rc38612-datasheet

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
11/21/2023 Version 1.1.1	
General Updates	Editorial updates only. No technical content changes.
09/27/2023 Version 1.1	
Initial public release.	N/A
12/09/2022 Version 1.0	
AMD Confidential. Initial release under NDA only.	N/A

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