

PRODUCT BRIEF

AMD ALVEO™ V80 COMPUTE ACCELERATOR CARD

For Big Data Sets and Memory-Intensive Workloads



OVERVIEW

Accelerate your memory-intensive workloads with the AMD Alveo™ V80 accelerator card. This flagship compute accelerator is architected for memory-bound applications that demand FPGA hardware adaptability to handle custom data types and custom data movement while scaling for large data sets at network line rates. Featuring a powerful AMD Versal™ HBM adaptive SoC, the card integrates HBM2e DRAM to overcome memory bottlenecks common in compute-intensive applications.

As a network-attached accelerator, the card features 4x200G connectivity for high-speed packet processing and compute clustering—all in a full-height, ¾ length dual-slot form factor. Scale your infrastructure to hundreds of accelerators over Ethernet or leverage the card's MCIO cable for clustering over PCIe®.

As a platform built for traditional FPGA developers, the Alveo V80 accelerator card is paired with the Alveo Versal Example Design (AVED) for ease of bring up using the AMD Vivado™ Design Suite.

HIGHLIGHTS

HARDWARE ADAPTABLE FOR MEMORY-BOUND WORKLOADS

- Massive parallelism and hardware adaptability for workload optimization
- HBM2e for memory-bound applications with large data sets

2X CAPABILITY VS. ALVEO U55C' COMPUTE ACCELERATOR

- 2X logic density and memory bandwidth
- 4X network bandwidth for packet processing and large-scale compute clustering

FAMILIAR DEVELOPMENT FLOWS FOR FPGA DESIGNERS

- Alveo Versal Example Design (AVED) for ease of hardware bring-up
- Support for Vivado Design Suite and traditional RTL flows

2X CAPABILITY OF THE ALVEO U55C' ACCELERATOR CARD

KEY APPLICATIONS

HIGH PERFORMANCE COMPUTING

- Genomic Sequencing
- Molecular Dynamics
- Radar Processing
- Sensor Processing
- Astrophysics

NETWORKING AND AI CONNECTIVITY

- Firewall
- Packet Monitoring
- GPU Clustering

FINTECH AND BLOCKCHAIN

- Risk Analysis
- Algorithmic Trading / Back Testing
- Web3 & Zero Knowledge Cryptography

STORAGE ACCELERATION

- Compression for Server Node Storage Arrays

DATABASE ACCELERATION AND ANALYTICS

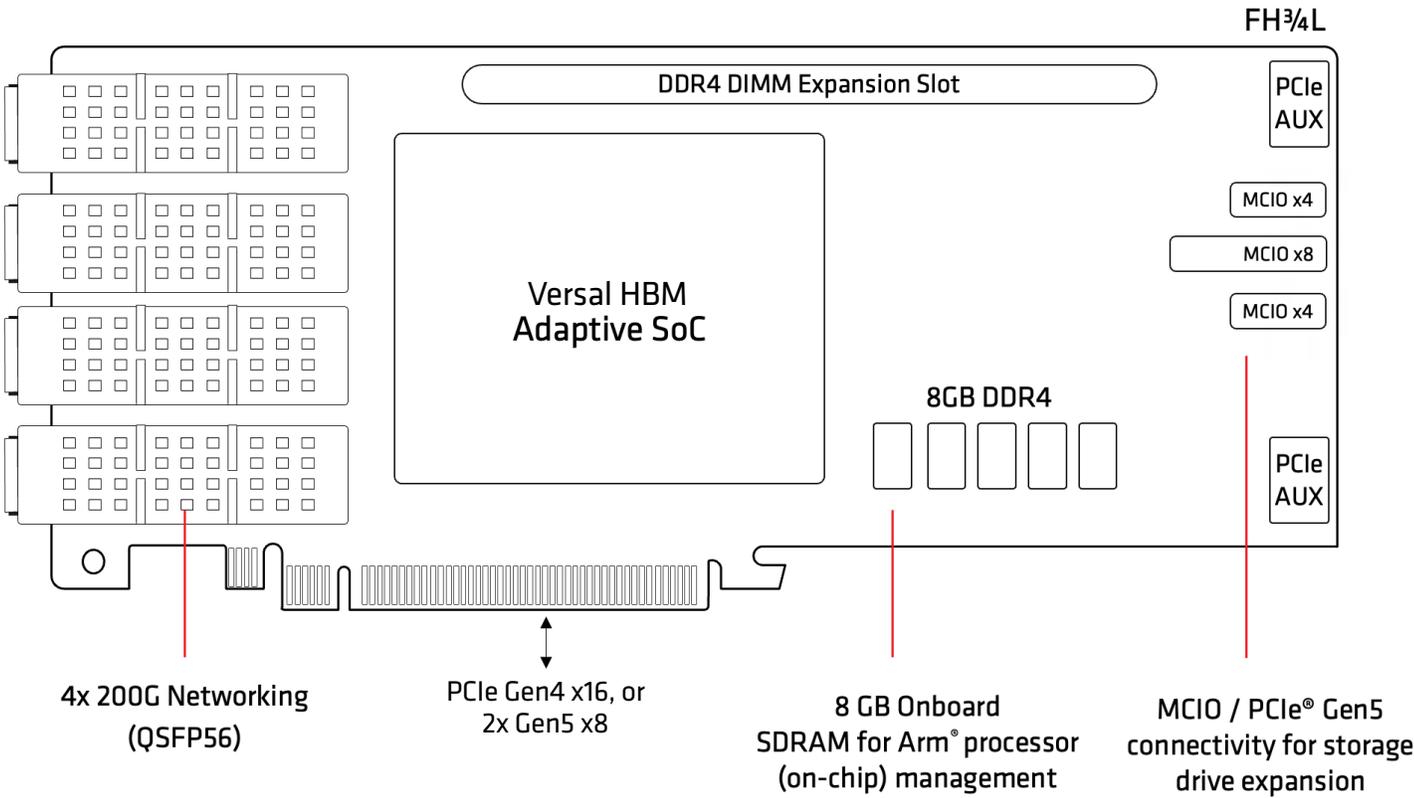
- Fraud Detection
- Public Sector
- Healthcare Analytics
- Supply Chain Analysis

HARDWARE ADAPTABLE FOR BIG DATA SETS AND MEMORY-INTENSIVE WORKLOADS

The Alveo V80 accelerator card is powered by a Versal HBM adaptive SoC device, featuring over 820 GB/s of high-bandwidth memory (HBM2e) to break through performance bottlenecks. The card also features 400G cryptographic engines for inline network monitoring and packet inspection, multi-hundred gigabit Ethernet core, and both 112G PAM4 and 32G NRZ transceivers for massive network bandwidth requirements.

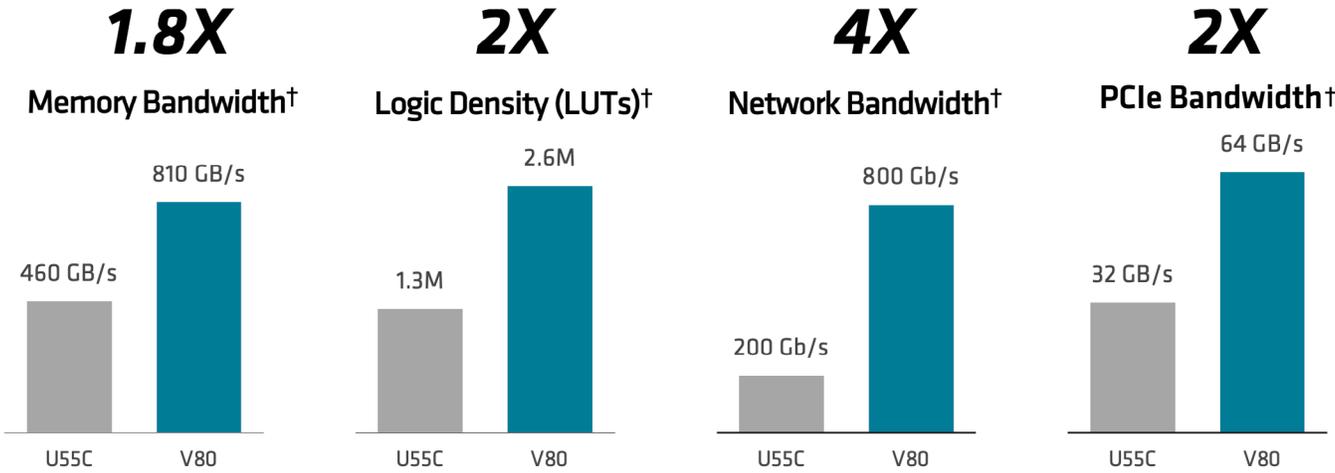
For scalability and compute clustering, the V80 accelerator card is optimized to maximize connectivity to network, CPU host, onboard memory, and NVMe storage drives. Respectively, the card integrates QSFP56 optical interfaces, PCIe Gen4 and Gen5 interfaces, DDR4 DIMM slots for memory expansion, and Mini Cool Edge I/O (MCIO) connectors to scale across compute and storage nodes at PCIe® Gen5 speeds.

ALVEO V80 ACCELERATOR CARD



2X CAPABILITY VS. PREVIOUS GENERATION ALVEO U55C ACCELERATOR CARD

As the flagship adaptable compute accelerator card from AMD, the Alveo™ V80 card provides a step-function increase in performance over its predecessor—the Alveo U55C Accelerator Card. With double the logic density, double the memory bandwidth, and 4X network bandwidth, the Alveo V80 card offers next-level performance benefits, power efficiency, and cost savings for more powerful clusters with fewer cards, servers, and rack space for equivalent compute.

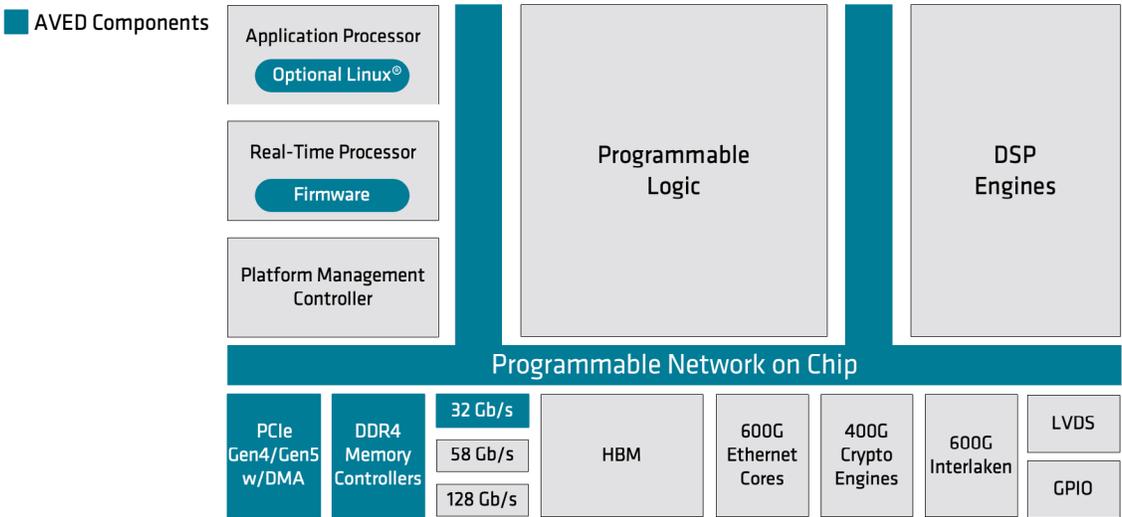


FAMILIAR DEVELOPMENT FLOWS FOR FPGA DESIGNERS

The Alveo V80 card is fully enabled for traditional hardware developers through the Alveo Versal Example Design, available on [GitHub](#). AVED is an FPGA design framework that simplifies hardware bring-up using traditional FPGA and RTL flows, based on the Vivado Design Suite.

The example design for Alveo hardware provides an efficient starting point using a pre-built PCIe subsystem implemented on the Versal HBM device, comprised of the integrated PCIe block with DMA engine, hardened memory controller, programmable network on chip, and basic self-test IP and firmware for system boot. The design ensures ease of card management, telemetry, and ease of access to interfaces from the CPU host. Overall, AVED provides a foundation for hardware developers to maximize the value of the Alveo V80 card for faster time to bring-up and production deployment.

AVED DESIGN IMPLEMENTED ON VERSAL HBM DEVICE



SPECIFICATIONS

ALVEO V80 COMPUTE ACCELERATOR	
Device Resources	<ul style="list-style-type: none"> • Features Versal HBM XCV80 adaptive SoC device • 2.6M Look-up tables (LUTs) • 10,848 DSP slices • 673 Mb of on-chip embedded memory (132 Mb block RAM, 541 Mb UltraRAM)
HBM Capacity	<ul style="list-style-type: none"> • 32 GB HBM2e DRAM (2x 16 GB stacks) • 820 GB/s peak bandwidth
Integrated Connectivity Cores	<ul style="list-style-type: none"> • 3x 400G High-Speed Crypto Engines supporting bulk crypto, IPsec, and MACsec¹ • 6x 100G Multirate Ethernet MAC¹ • 3x 600G Ethernet MAC • 1x 600G Interlaken
Processing Subsystem	<ul style="list-style-type: none"> • Dual-core Arm® Cortex®-A72 application processor • Dual-core Arm Cortex-R5F real-time processor • Platform management controller
Onboard Memory	<ul style="list-style-type: none"> • 8 GB of onboard SDRAM for Arm processor management
Supported Tools	<ul style="list-style-type: none"> • AMD Vivado Design Suite • AMD Alveo Versal Example Design
PCIe Interface and Expansion	<ul style="list-style-type: none"> • PCIe Gen4 x16 or 2x Gen5 x8 • Mini Cool-Edge I/O (MCIO) expansion connectors over PCIe Gen5
Transceivers	<ul style="list-style-type: none"> • 68 GTYP transceivers (32.75 Gb/s) • 60x (56 Gb/s) or 30x (112 Gb/s) GTM PAM4 transceivers
Memory Expansion	<ul style="list-style-type: none"> • 32 GB DDR4 expansion DIMM
Network Interfaces	<ul style="list-style-type: none"> • 4x QSFP56 optical ports (2x 100G or 4x 10/25/40/50G per port)
Form Factor	<ul style="list-style-type: none"> • Full-Height, ¾ Length (FH¾L) • Dual-slot
Power and Thermal²	<ul style="list-style-type: none"> • 190W TDP, passive cooling
Product SKU	<ul style="list-style-type: none"> • A-V80-P64G-PQ-G

NEXT STEPS

- To learn more, visit www.amd.com/v80
- To purchase, contact your local sales representative, or visit www.amd.com/v80 and complete the **Product Inquiry form**
- To download the Vivado Design Suite, visit the **download page**
- To download AVED and access documentation, visit **GitHub**
- All other questions, email dc_inquiries@amd.com

ENDNOTES

† Based on AMD comparison of the specifications in the publicly available AMD Alveo Product Selection Guide as of April, 2024. ALV-13.

1: Aggregate throughput of High-Speed Crypto Engines (3x 400G) and Ethernet MAC (3x 600G) refer to device capability and not indicative of total throughput via network ports

2: Total thermal power (TDP) is device and server dependent

DISCLAIMERS

The information contained herein is for informational purposes only and is subject to change without notice. While every precaution has been taken in the preparation of this document, it may contain technical inaccuracies, omissions and typographical errors, and AMD is under no obligation to update or otherwise correct this information. Advanced Micro Devices, Inc. makes no representations or warranties with respect to the accuracy or completeness of the contents of this document, and assumes no liability of any kind, including the implied warranties of noninfringement, merchantability or fitness for particular purposes, with respect to the operation or use of AMD hardware, software or other products described herein. No license, including implied or arising by estoppel, to any intellectual property rights is granted by this document. Terms and limitations applicable to the purchase or use of AMD's products are as set forth in a signed agreement between the parties or in AMD's Standard Terms and Conditions of Sale. GD-18

COPYRIGHT NOTICE

© Copyright 2024 Advanced Micro Devices, Inc. AMD, the AMD Arrow logo, Alveo, Versal, Vivado, and combinations thereof are trademarks of Advanced Micro Devices, Inc. AMBA, AMBA Designer, Arm, ARM1176JZ-S, CoreSight, Cortex, PrimeCell, Mali, and MPCore are trademarks of Arm Limited in the EU and other countries. Linux® is the registered trademark of Linus Torvalds in the U.S. and other countries. PCI, PCIe, and PCI Express are trademarks of PCI-SIG and used under license. Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies. All other trademarks are the property of their respective owners. PID2645905